

FIG. 1

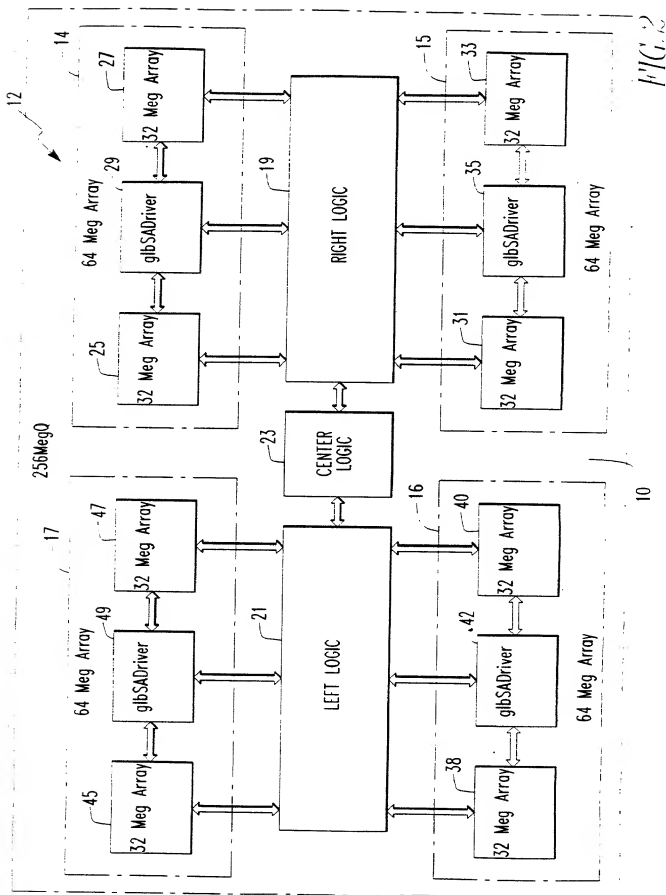
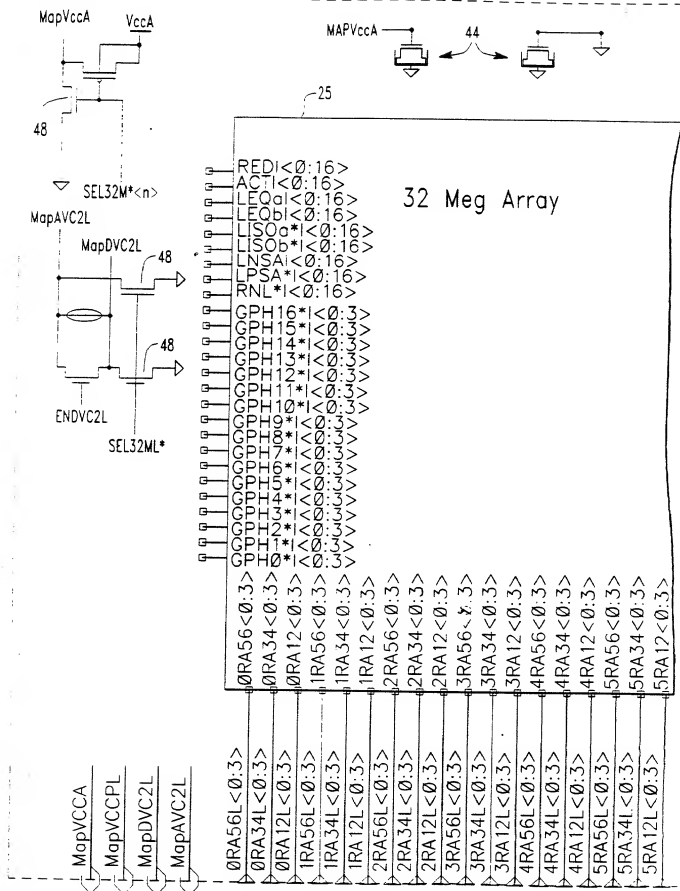
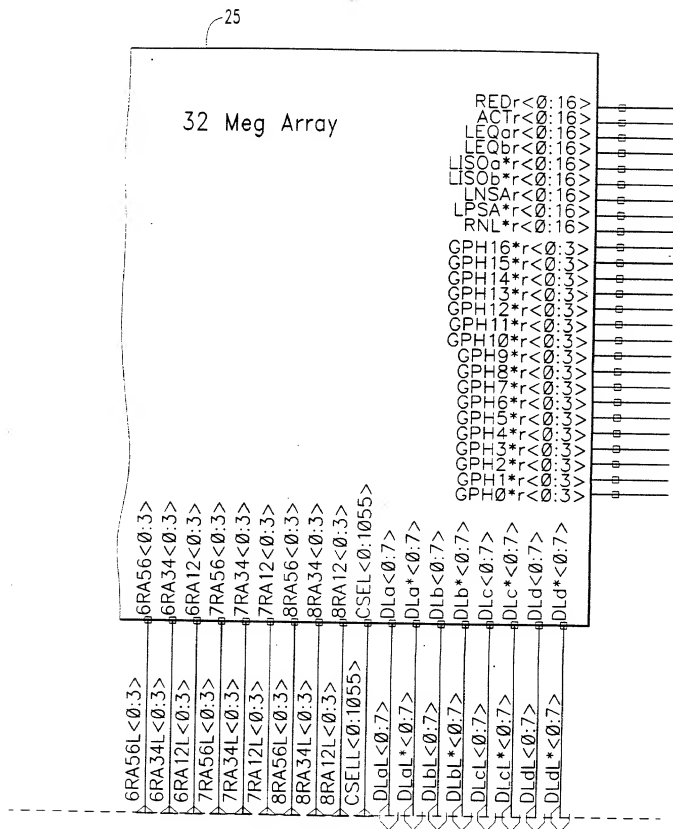


FIG. 2

3,367





-29

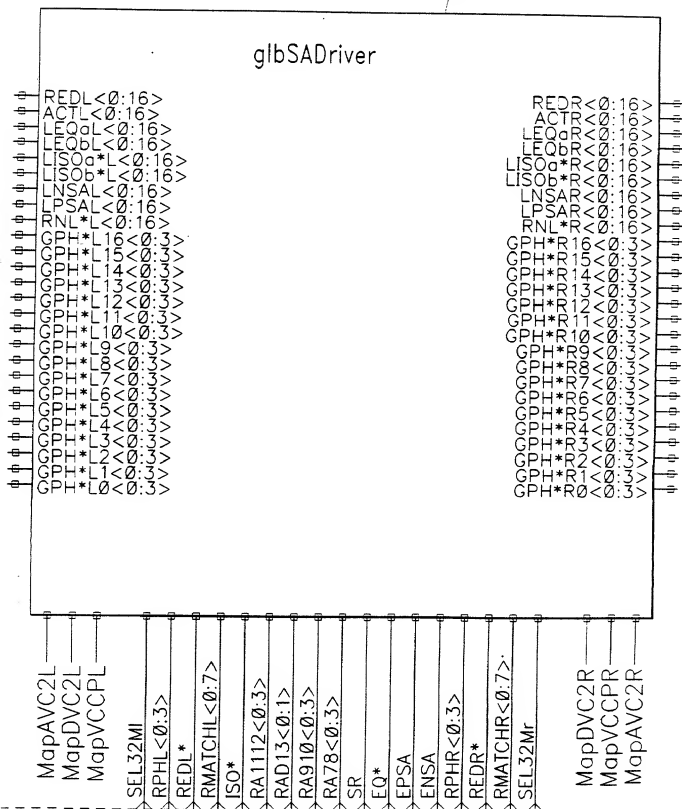
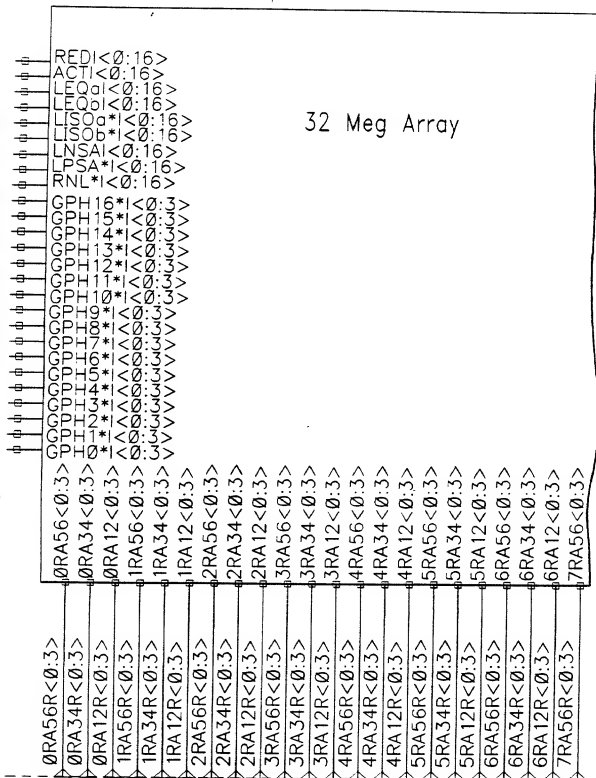


FIG. 3D

6, 367

27

32 Meg Array



7/367

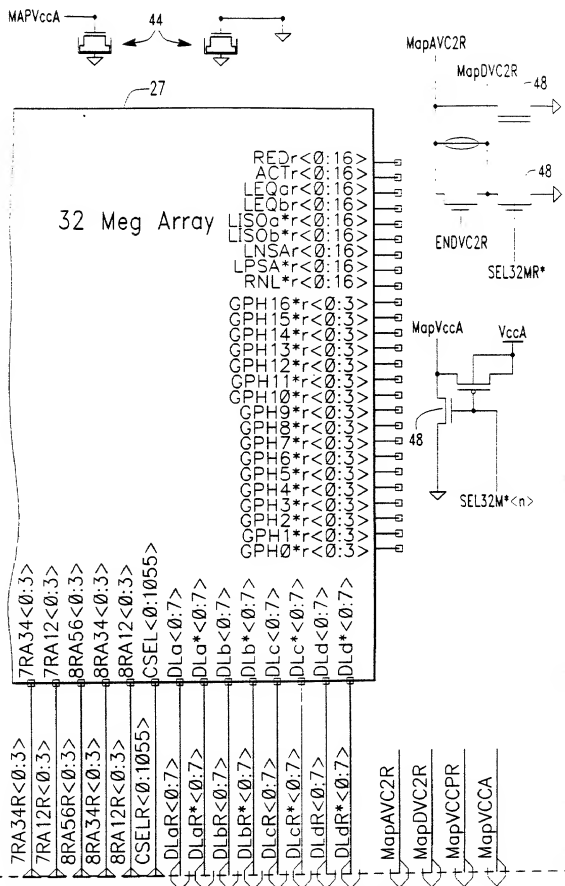


FIG. 5 is a schematic diagram of a memory array structure. The diagram shows a grid of 256K arrays (50) connected to sense amplifiers (52) and multiplexers (55). The array is organized into rows and columns. Labels include: 50 (array), 25 (row decoder), 50 (array), 50 (array), SENSE AMPLIFIERS, 52, SEE FIG. 5, ROW DECODERS, 54, and MULTIPLEXERS, 55.

FIG. 4

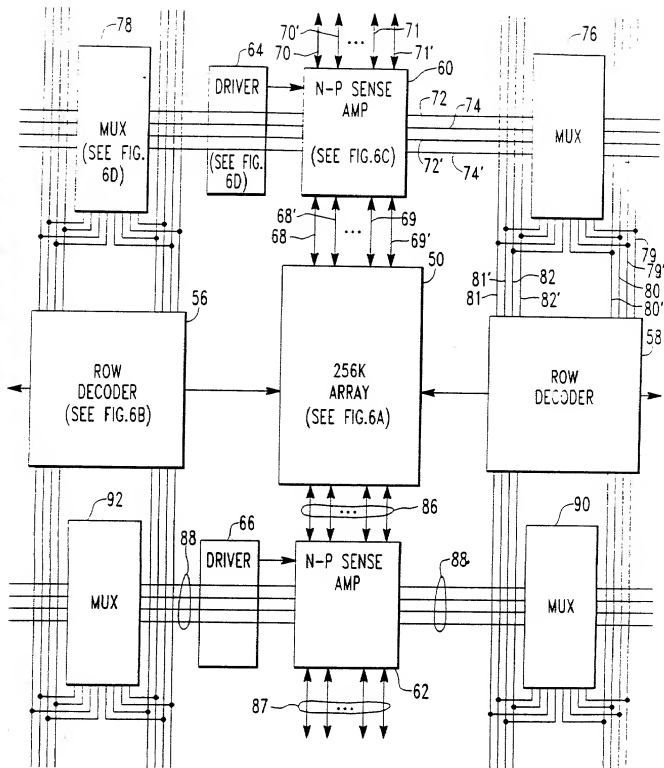


FIG. 5

10/367

TO N-P SENSE AMP 60

68

68'

69

69'

50

D1

D1*

D3

D3*

RDUM<0>

RWL<0>

RWL<1>

WL<3:251:4>

WL<0:252:4>

WL<1:253:4>

WL<2:254:4>

WL<255>

RDUM<1>

r516x4

M=1X

RDUM<2>

WL<256>

WL<257:

509:4>

WL<258:

510:4>

WL<259:

511:4>

WL<260:508:

4>RWL<2>

RWL<3>

RDUM<3>

D0

D0*

D2

D2*

87

TO N-P SENSE AMP 62

TO ROW
DECODER
56

TO ROW
DECODER
58

84

FIG. 6A

DATA LINES

11/367

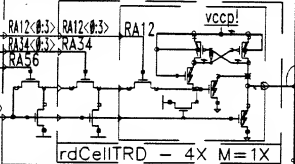
DATA LINES

56

96

97

4rdCellTRD = 4X M=1X



4rdCellTRD M=1X hspLOAD

4rdCellTRD M=1X hspLOAD

4rdCellTRD M=1X

4rdCellTRD M=1X

4rdCellTRD M=1X

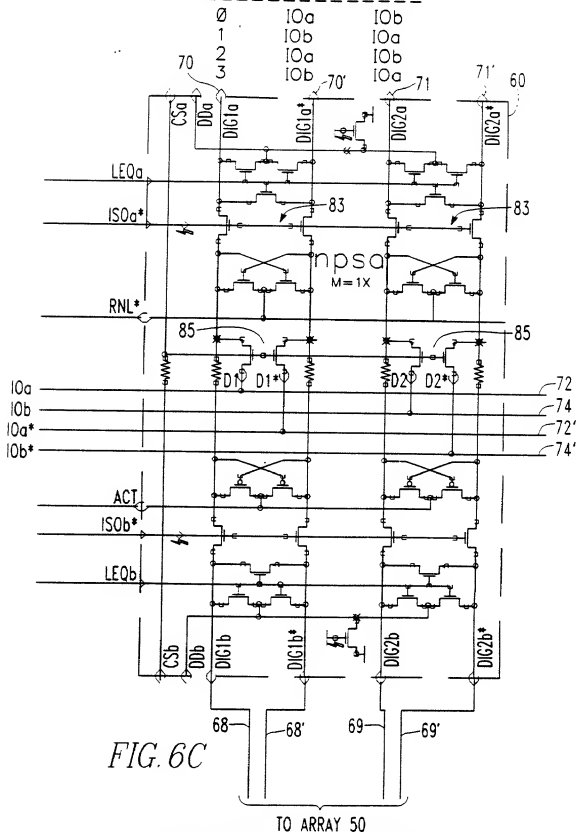
4rdCellTRD M=1X

4rdCellTRD M=1X

FIG. 6B

12,367

Connections of odd/even
columns to IOa and IOb
alternates with odd/even
column select lines:
CA01* D1(even) D2(odd)



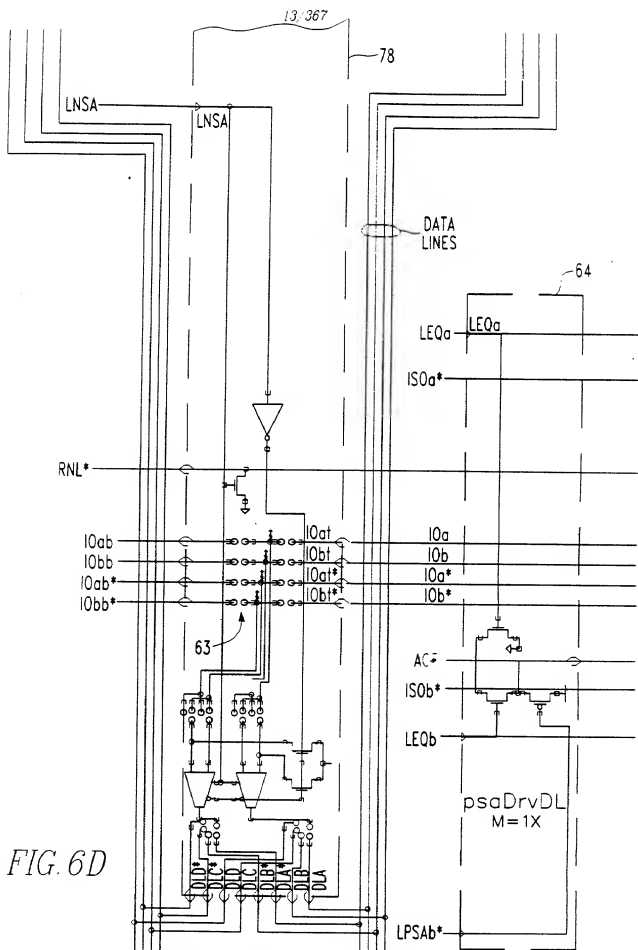


FIG. 6D

25

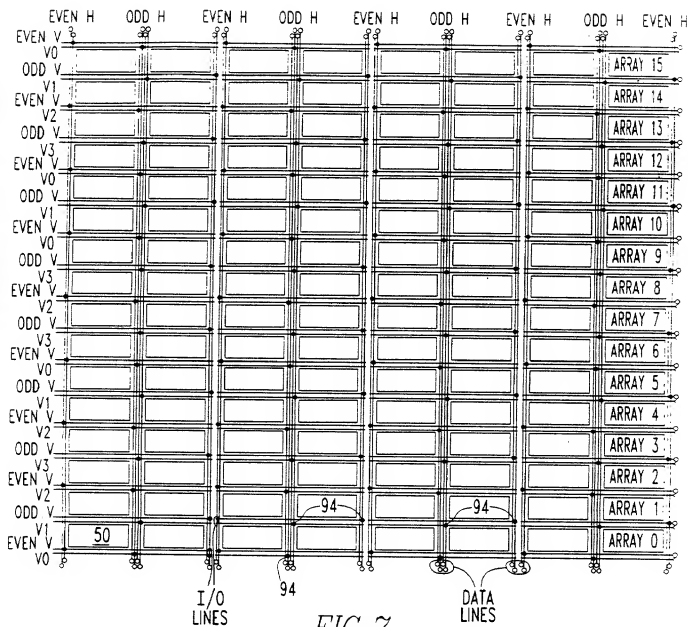


FIG. 7

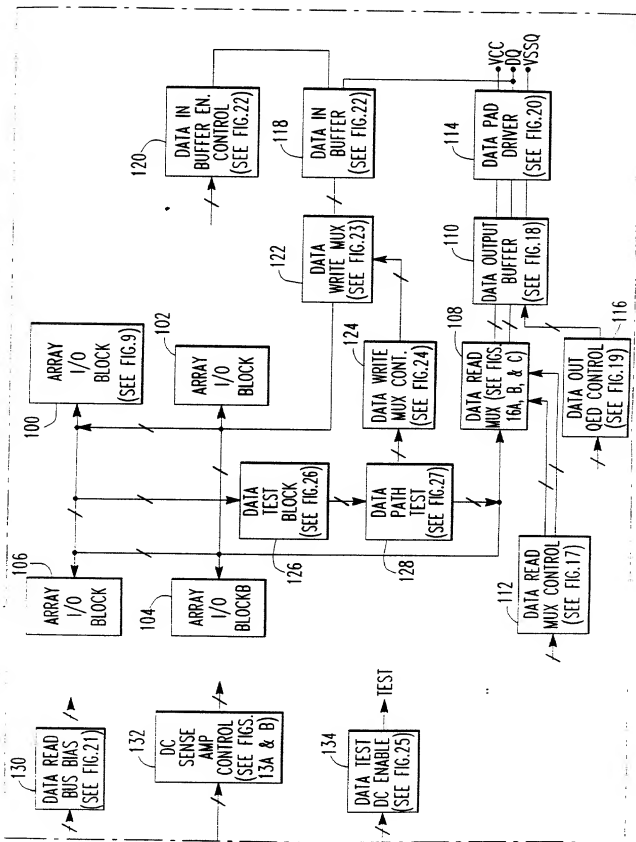


FIG. 8

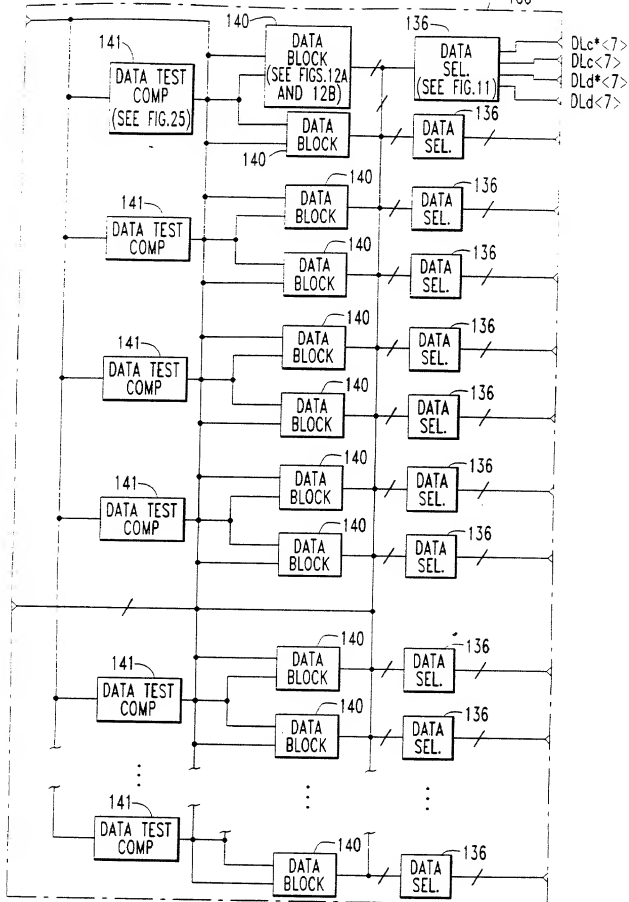
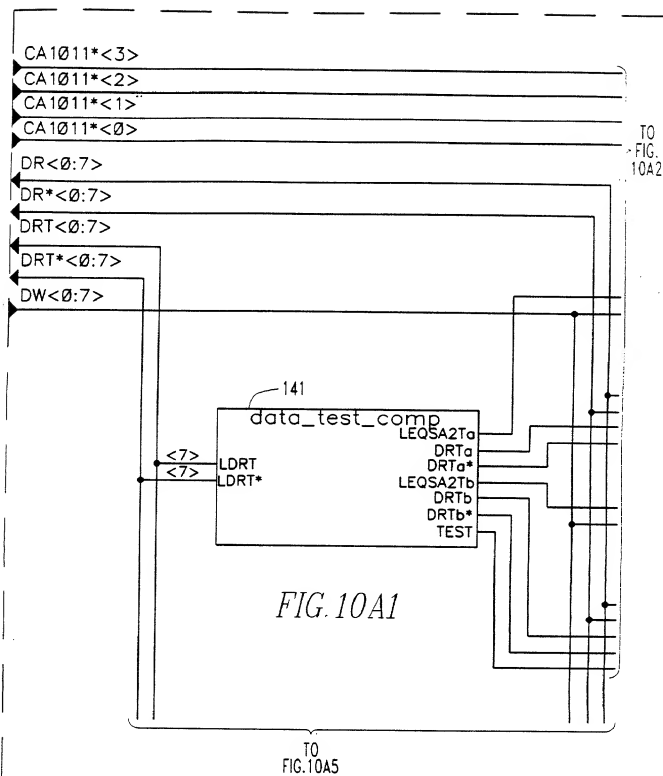


FIG. 9



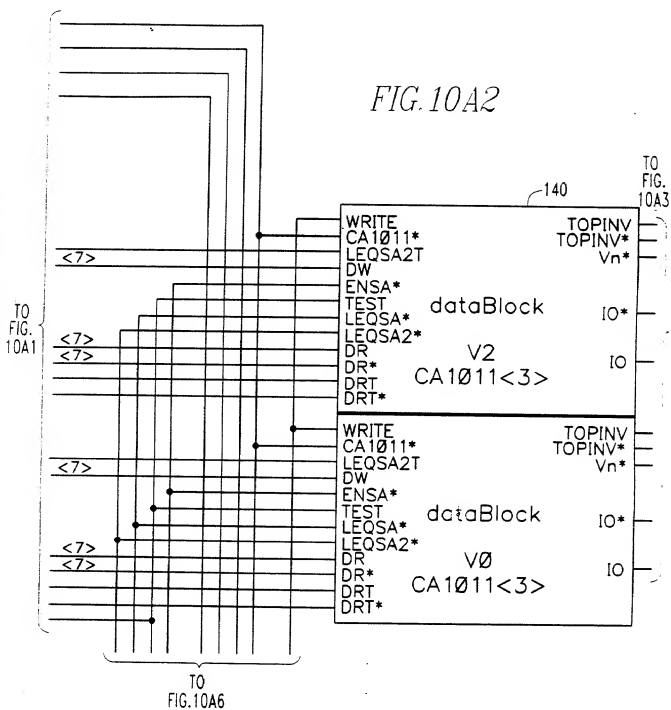
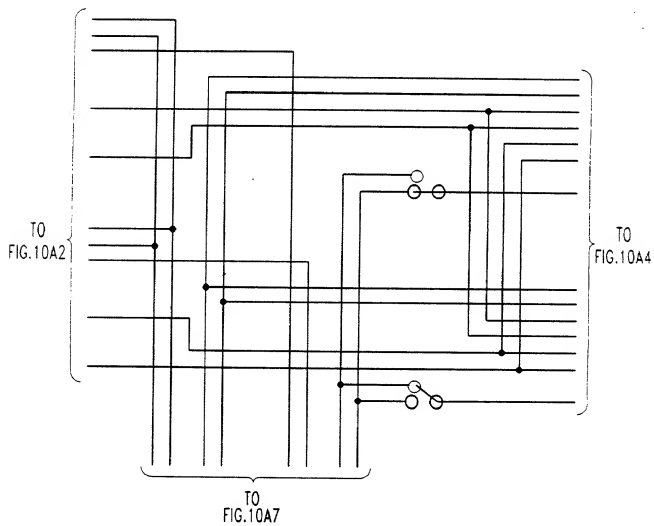


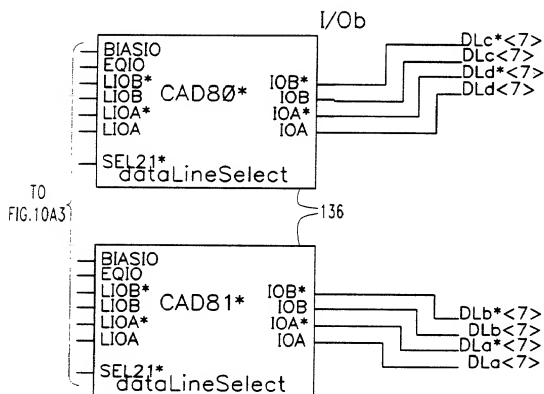
FIG. 10A3



arrayIOBlock

100

FIG. 10A4



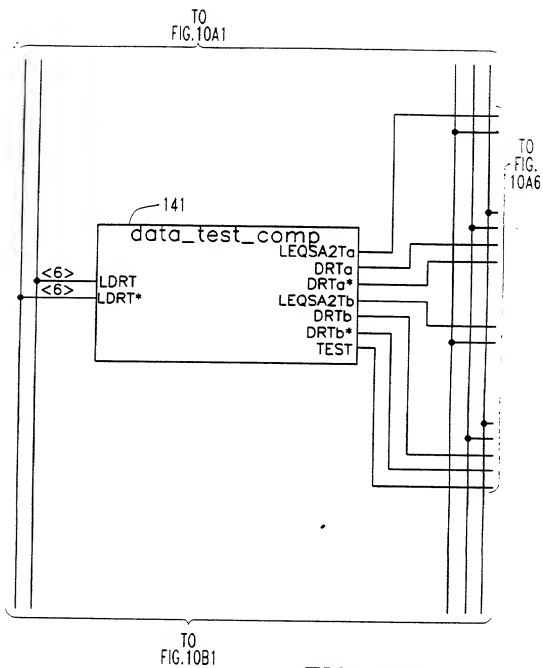


FIG. 10A5

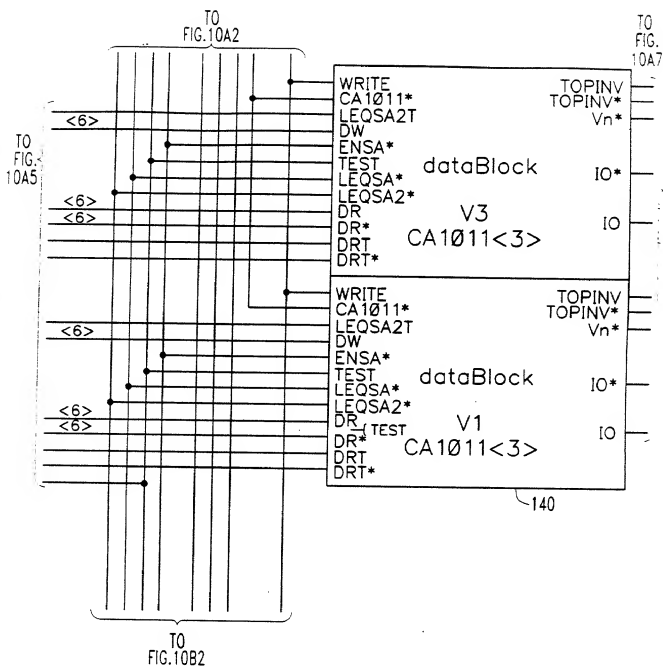


FIG. 10A6

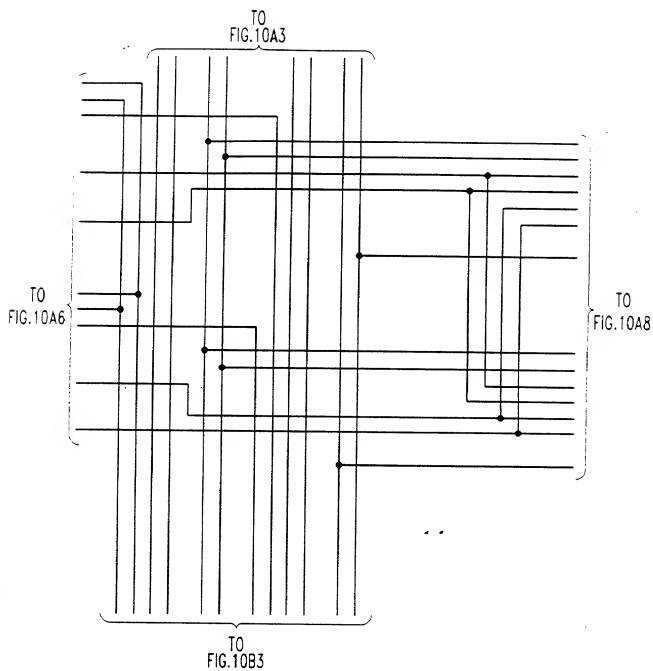


FIG. 10A7

I/Oa

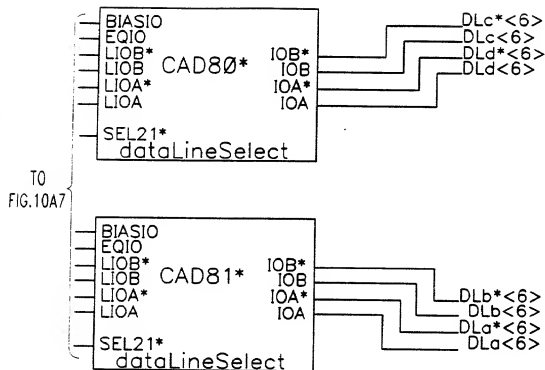


FIG. 10A8

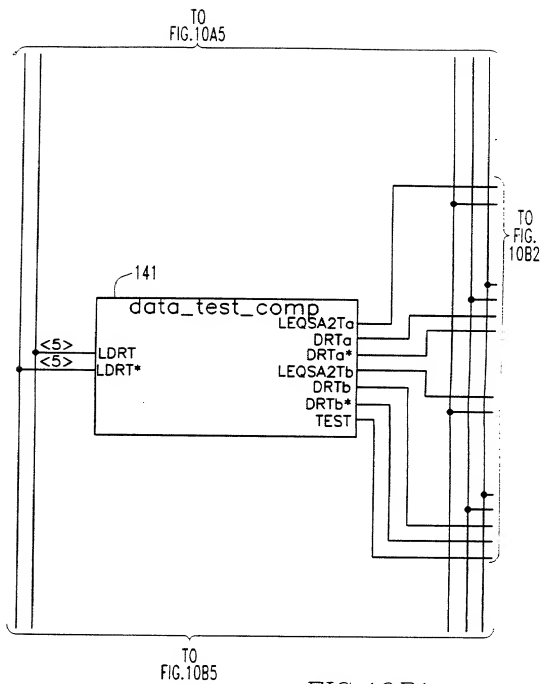


FIG. 10B1

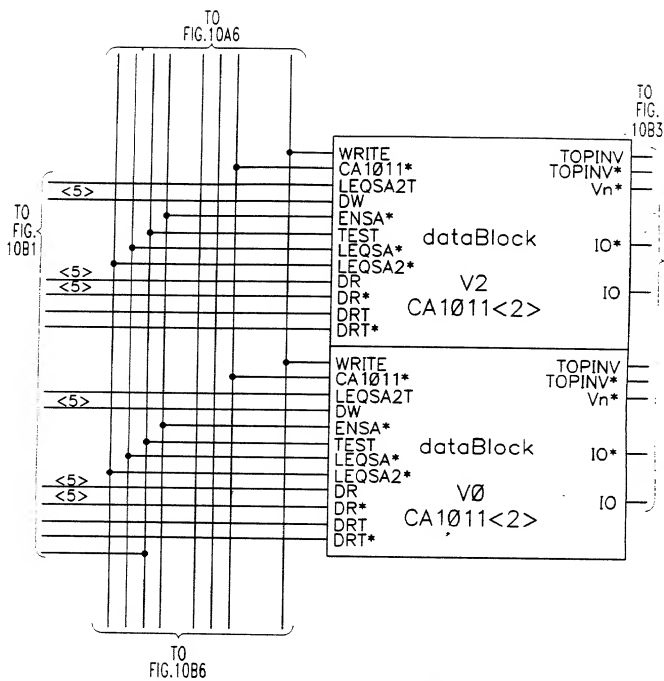


FIG. 10B2

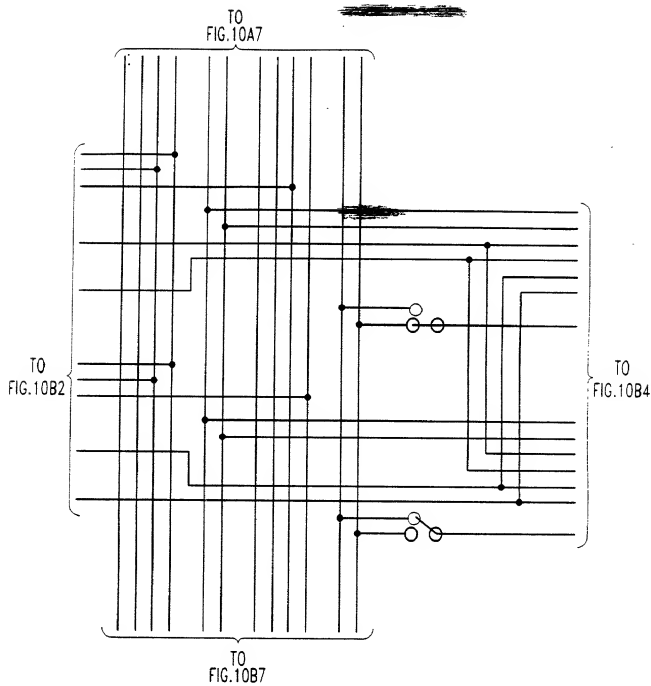


FIG. 10B3

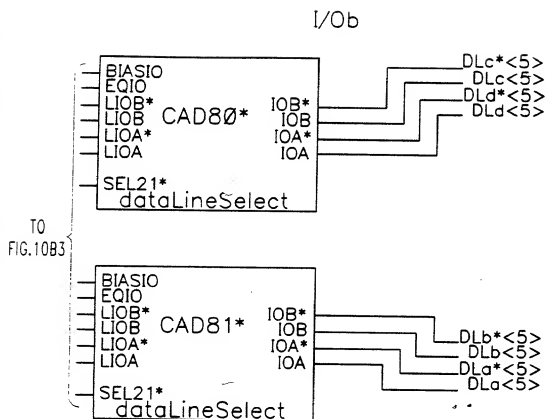


FIG.10B4

FIG. 10B5

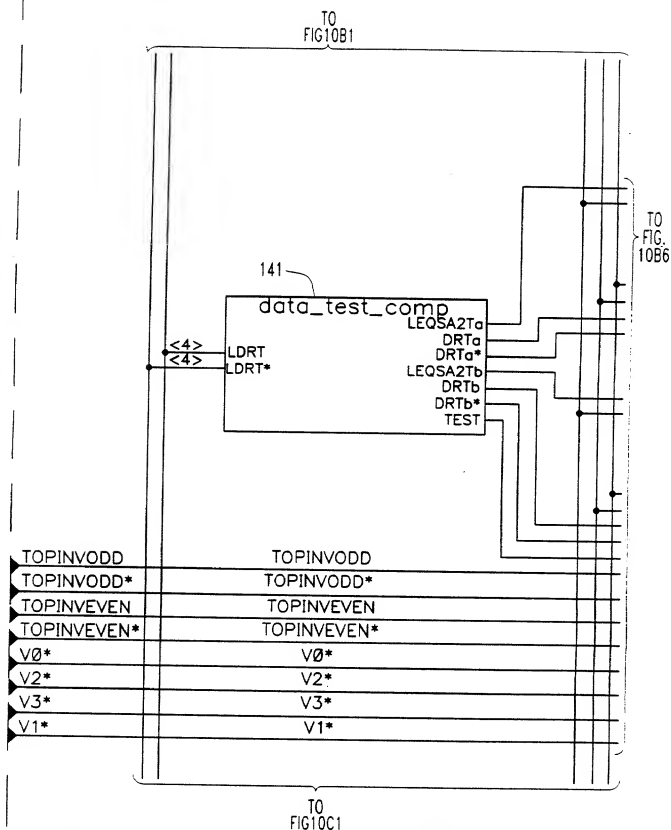


FIG. 10B6

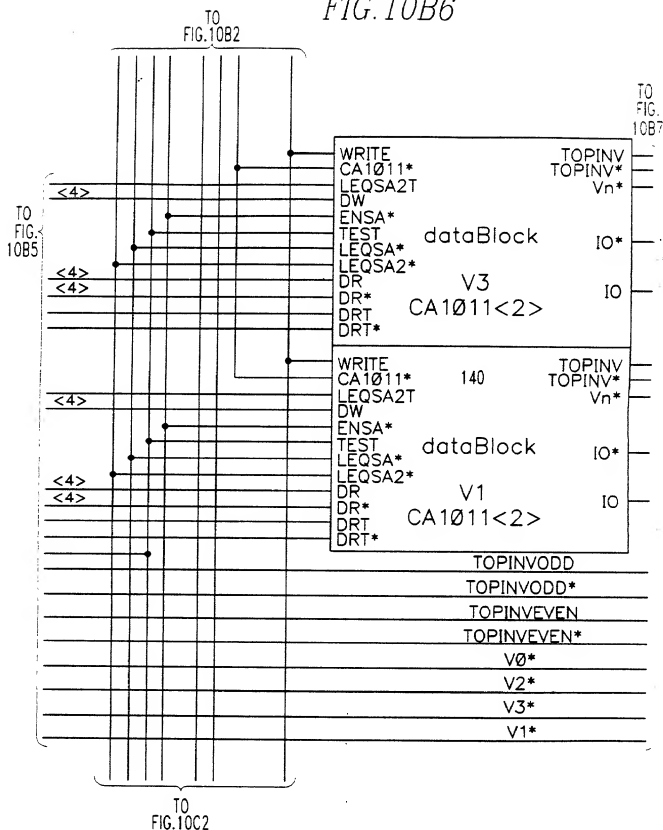


FIG. 10B3

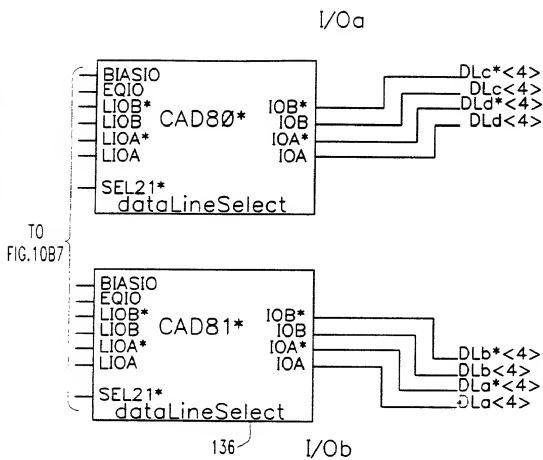
TO FIG. 10B6

TO FIG. 10B8

TO FIG. 10C3

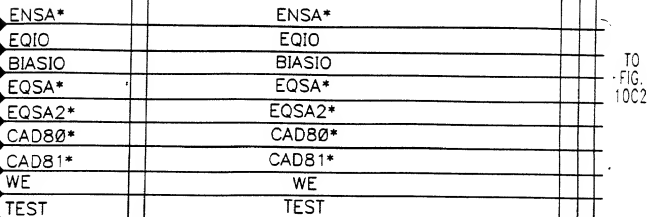
TO
FIG10C3

FIG. 10B8



33/367

TO
FIG.10B5



141

data_test_comp

<3>

LDRT
LDRT*

LEQSA2Ta
DRTa
DRTa*
LEQSA2Tb
DRTb
DRTb*
TEST

TO
FIG.10C5

FIG.10C1

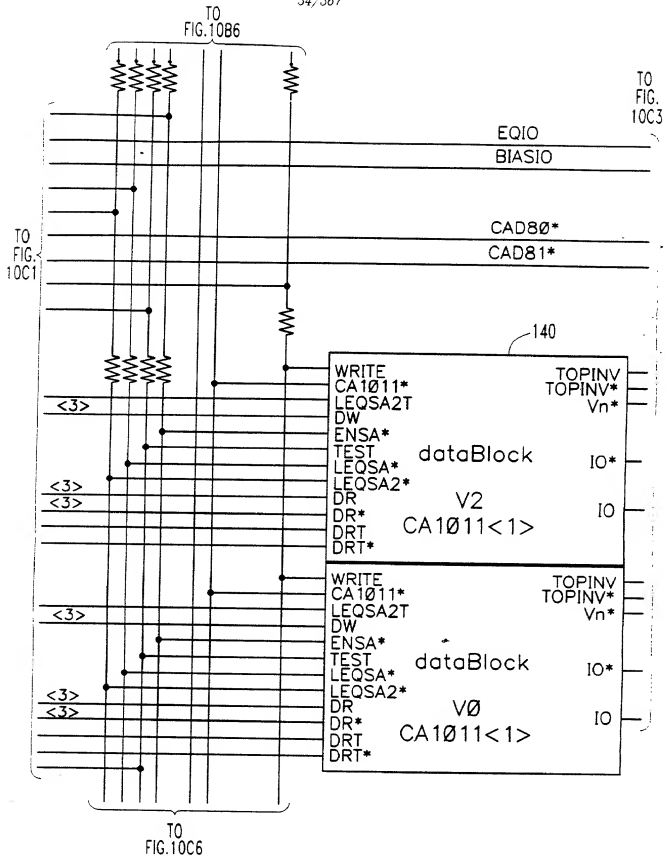


FIG. 10C2

35/367

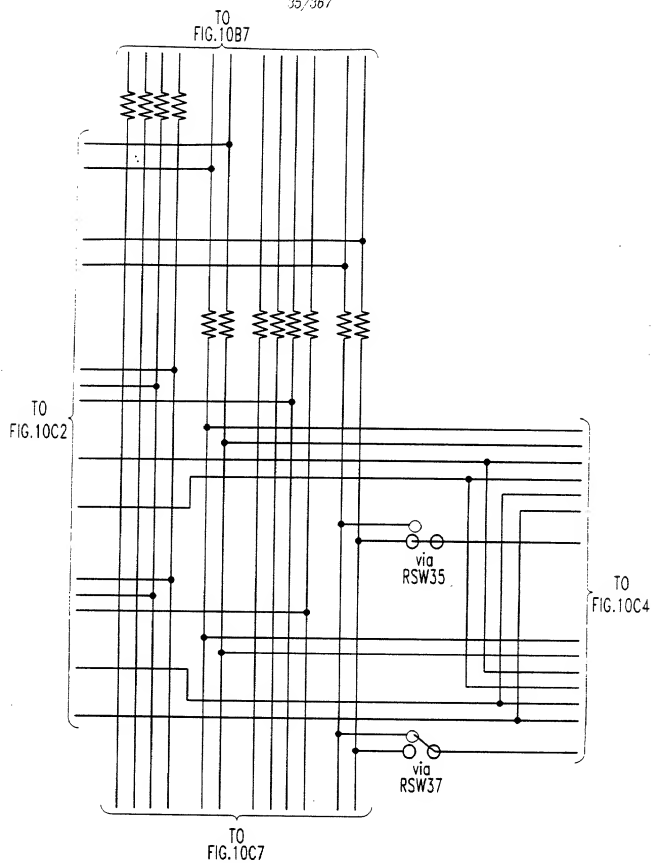
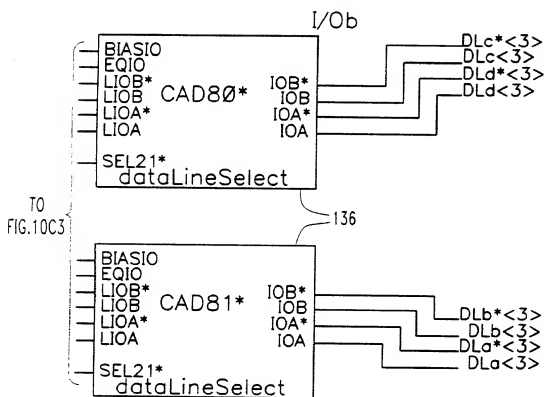


FIG. 10C3

FIG. 10C4



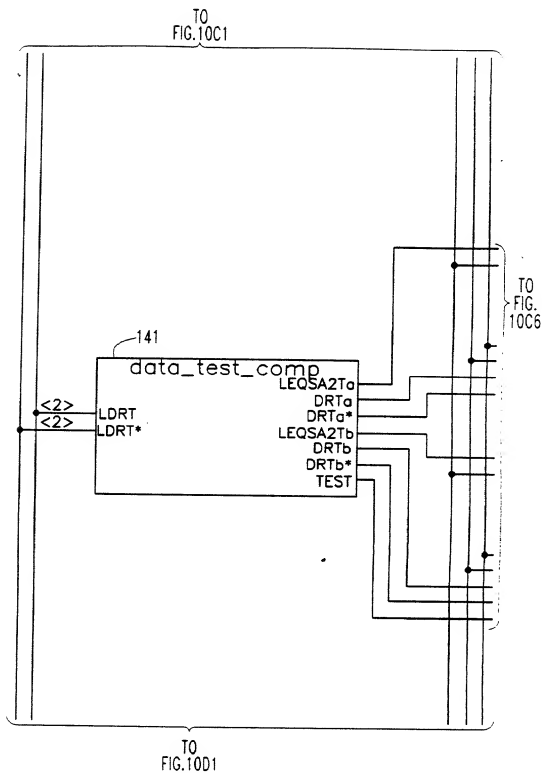


FIG. 10C5

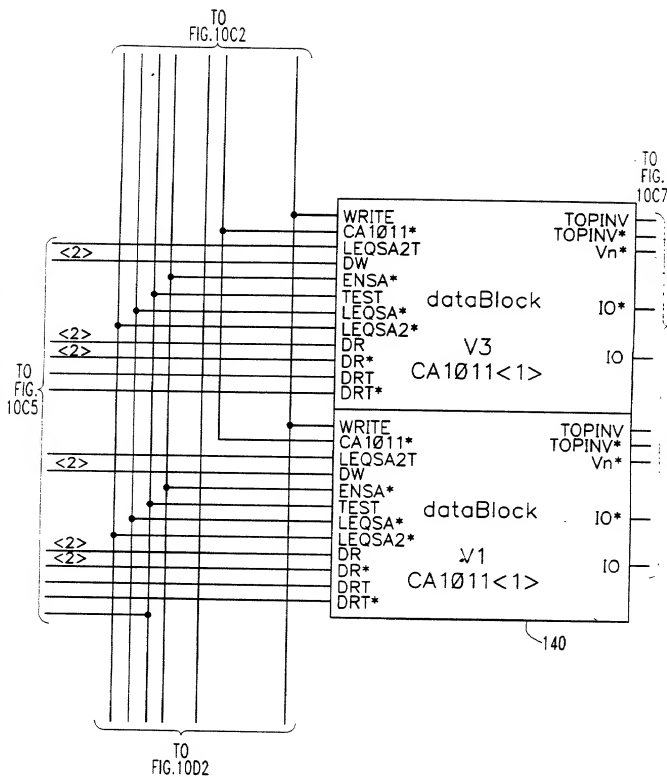


FIG. 10C6

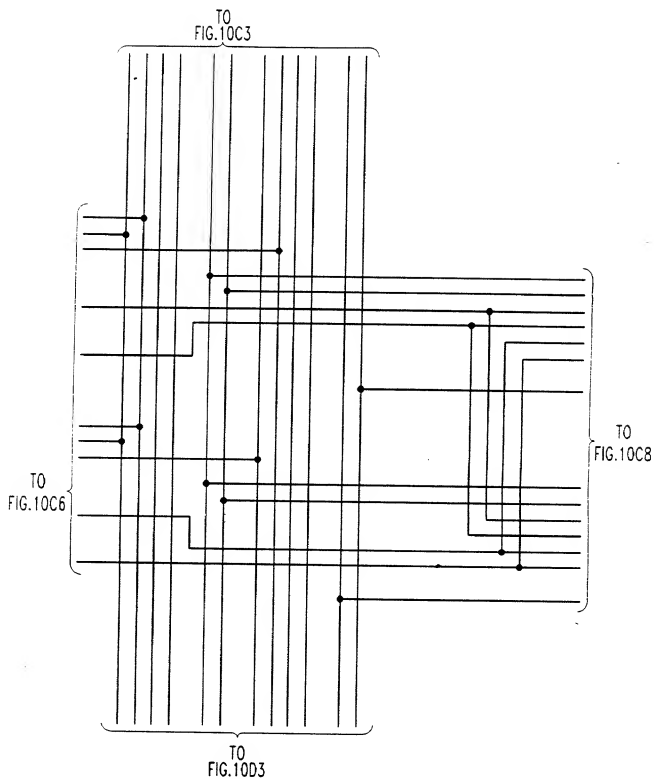


FIG. 10C7

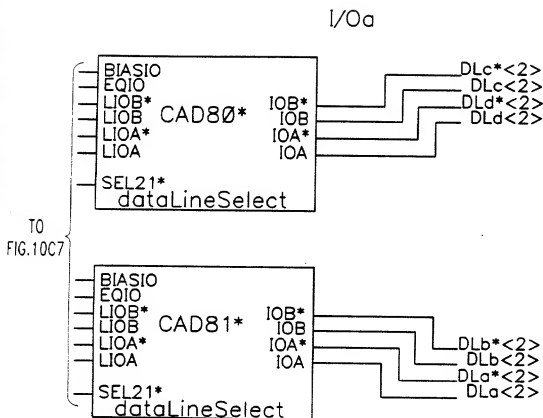


FIG. 10C8

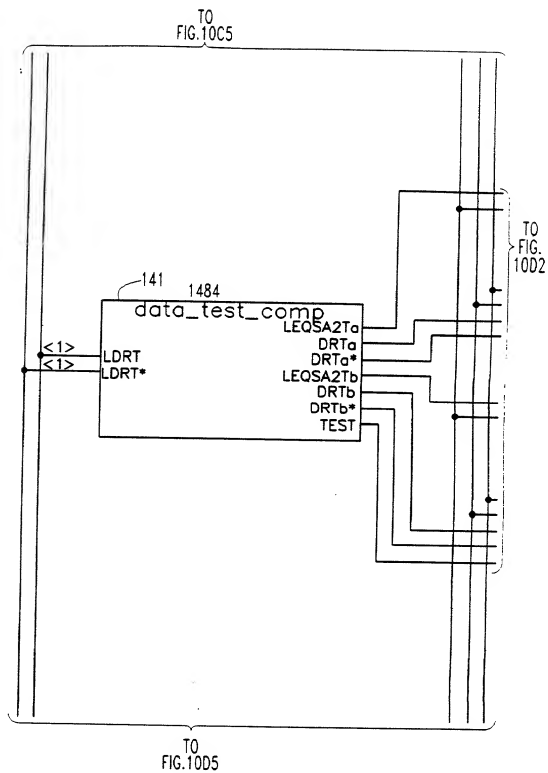


FIG. 10D1

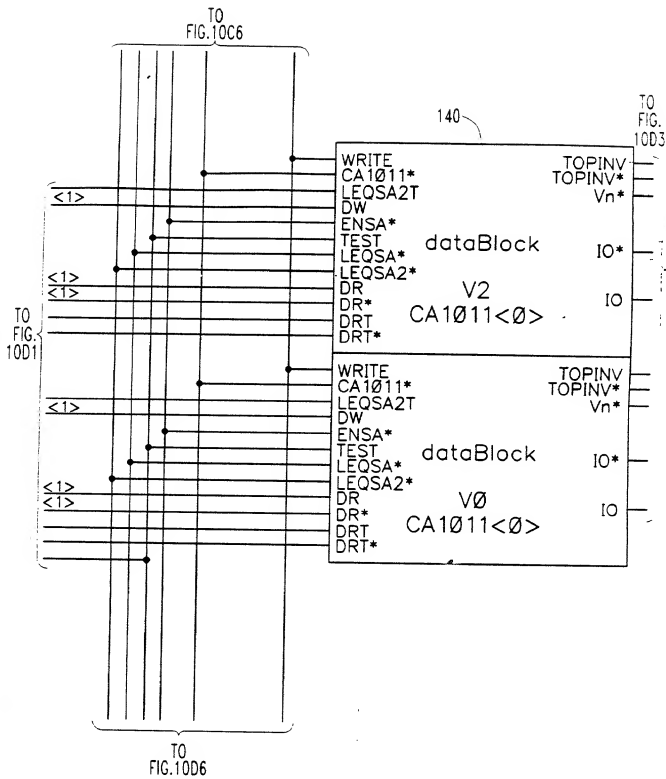
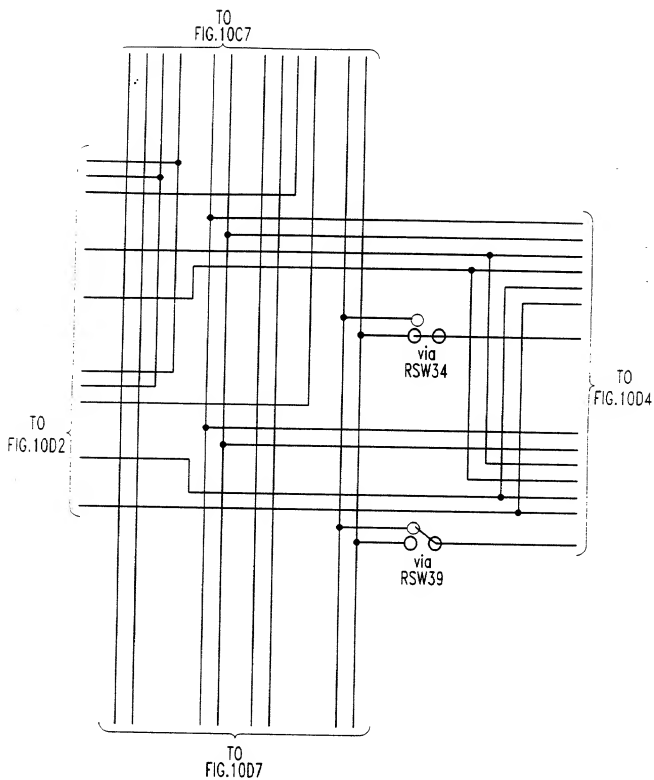


FIG. 10D2

*FIG. 10D3*

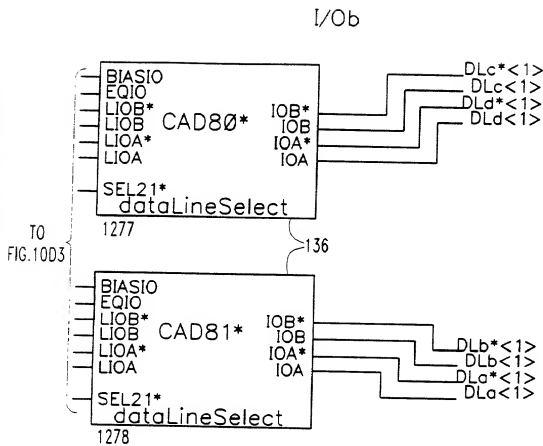


FIG. 10D4

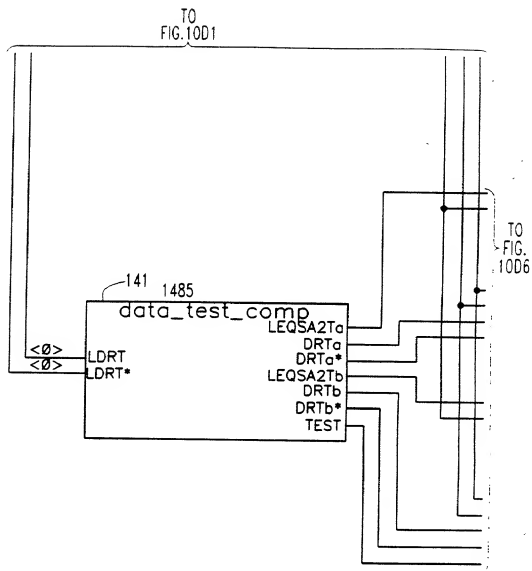


FIG. 10D5

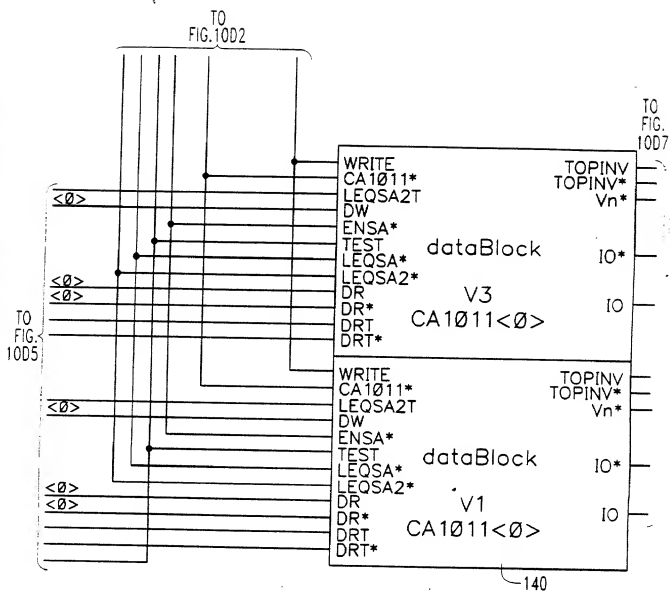


FIG. 10D6

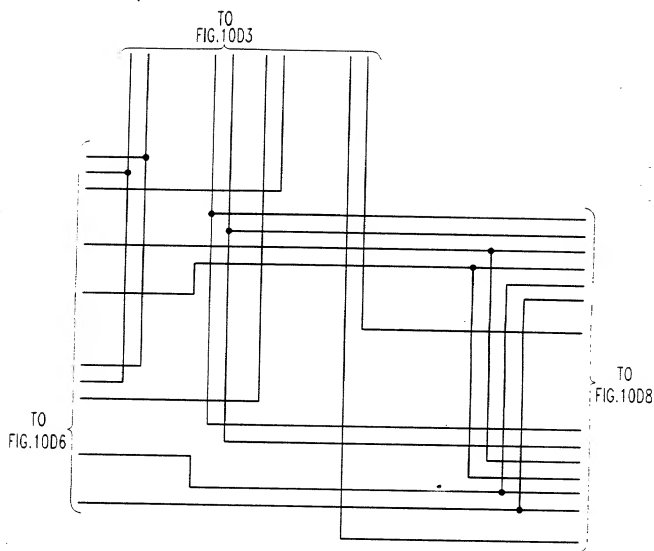


FIG.10D7

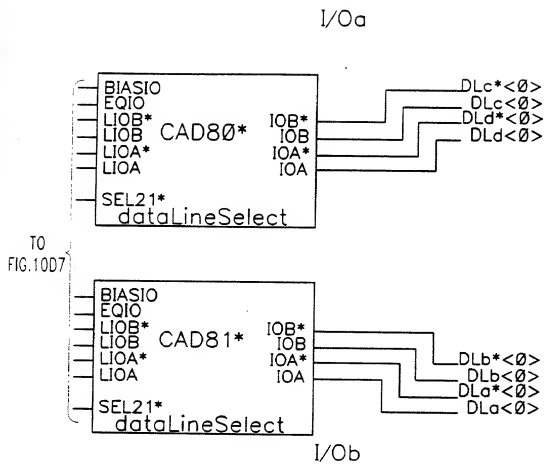


FIG.10D8

LIOA

LIO

dataBias2

LIOA*

LIO*

SEL21*

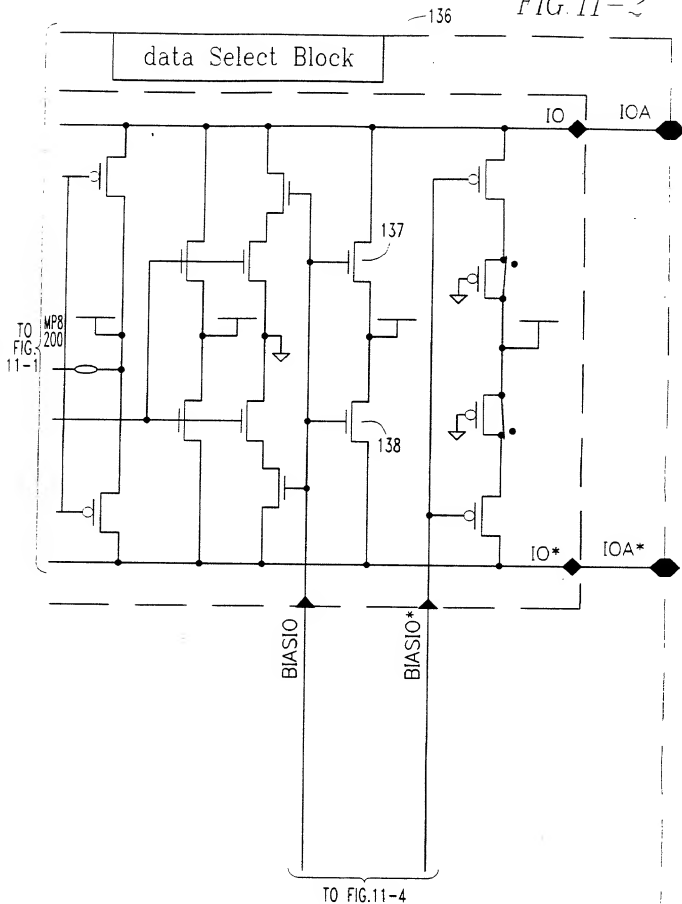
EQIO

EQIO*

TO
FIG.
11-2

TO FIG.11-3

FIG. 11-2



51.367

TO FIG.11-1

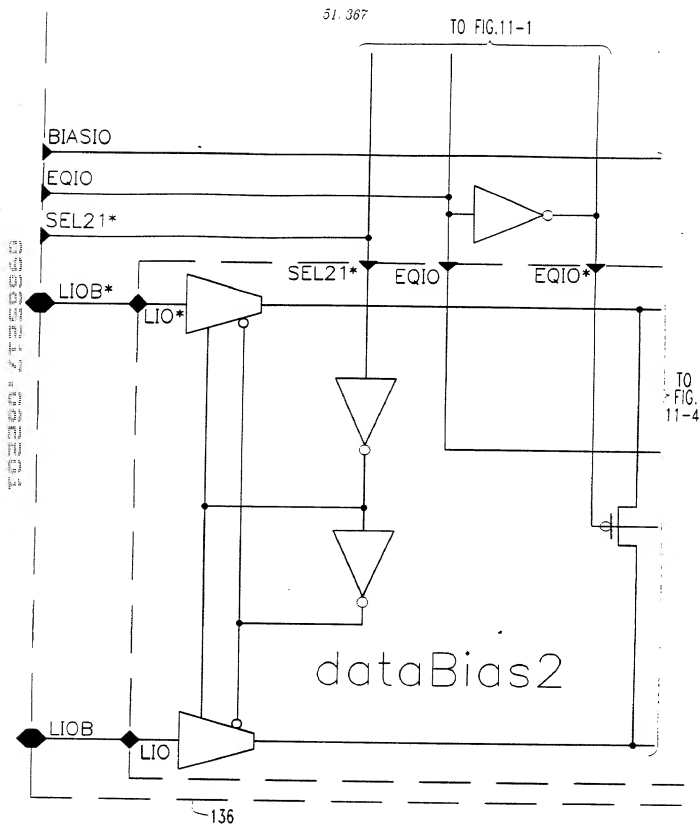


FIG.11-3

52/367

TO FIG. 11-2

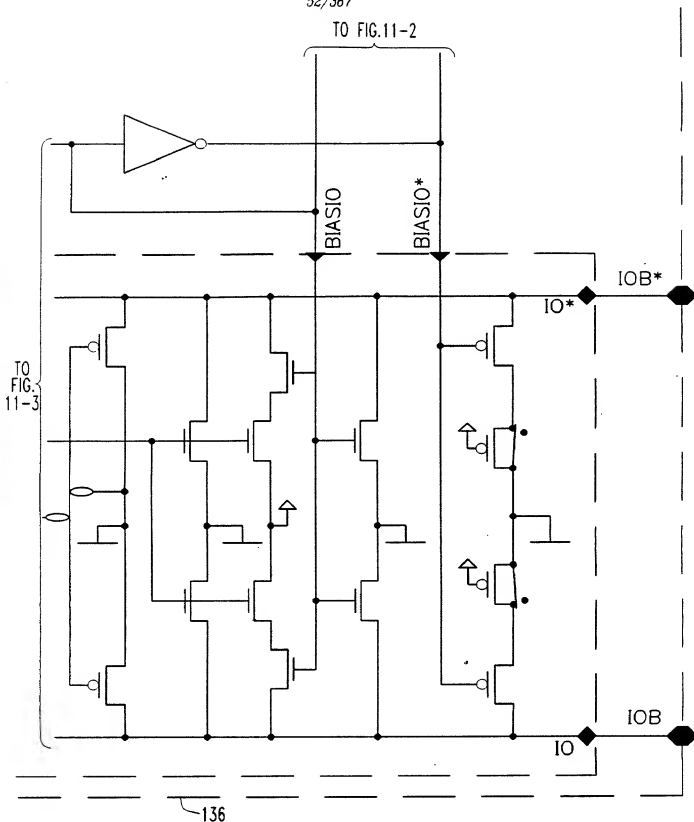
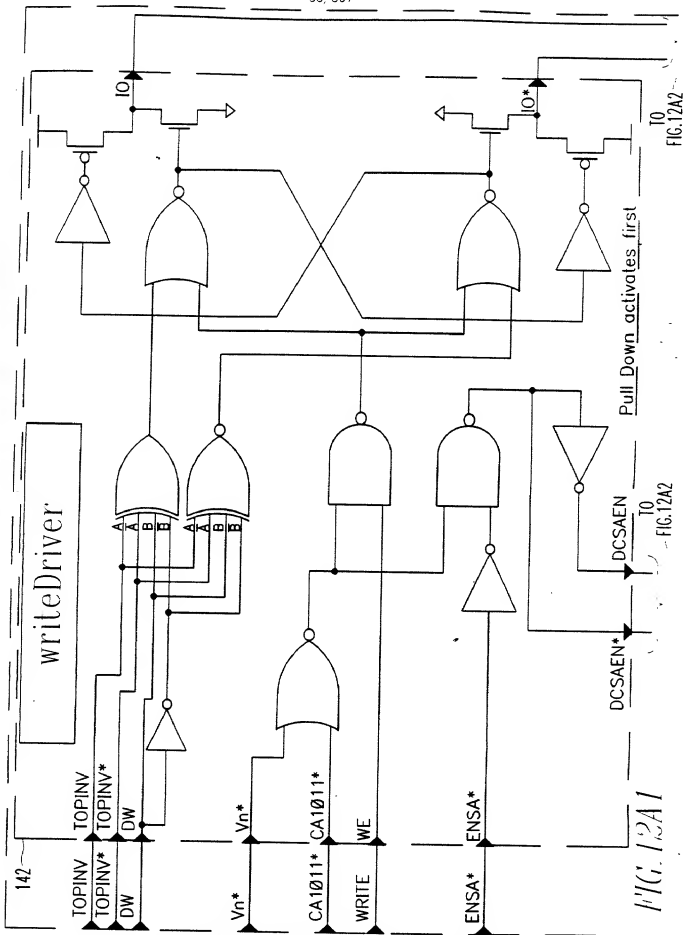


FIG. 11-4



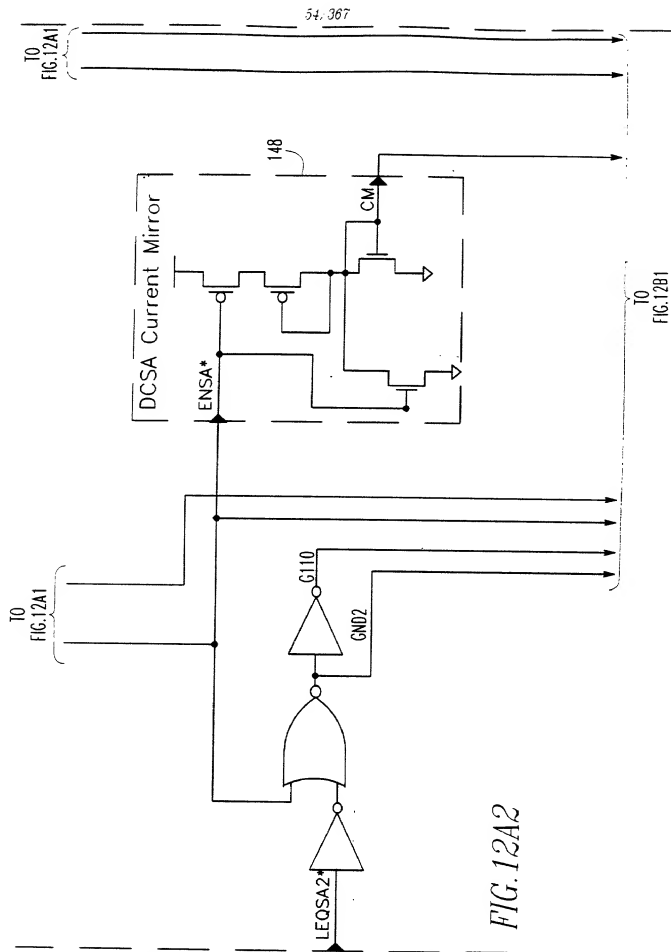


FIG. 12B1

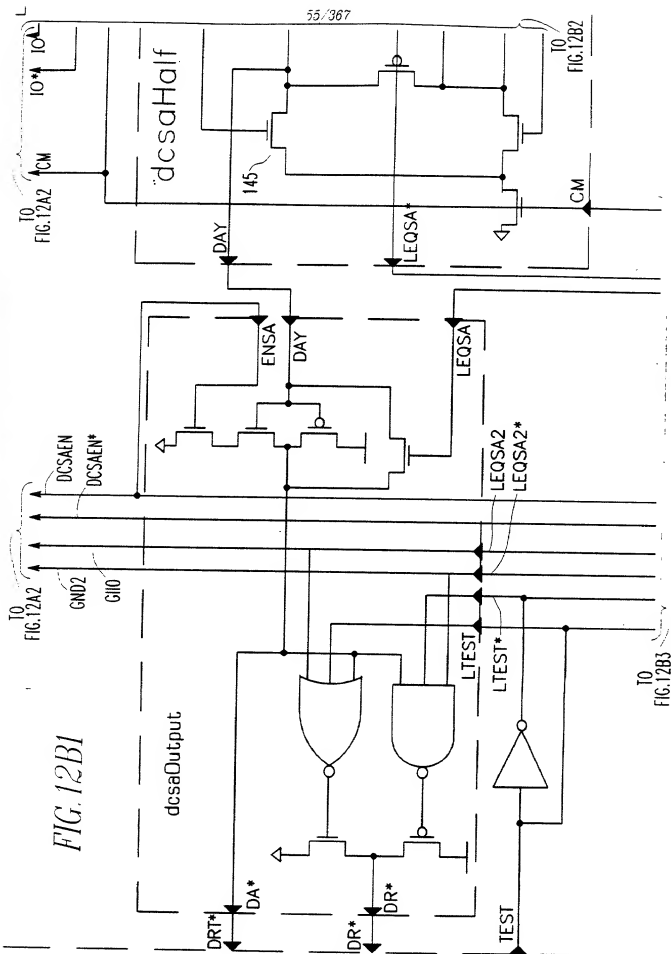


FIG. 12B3

FIG. 12B2

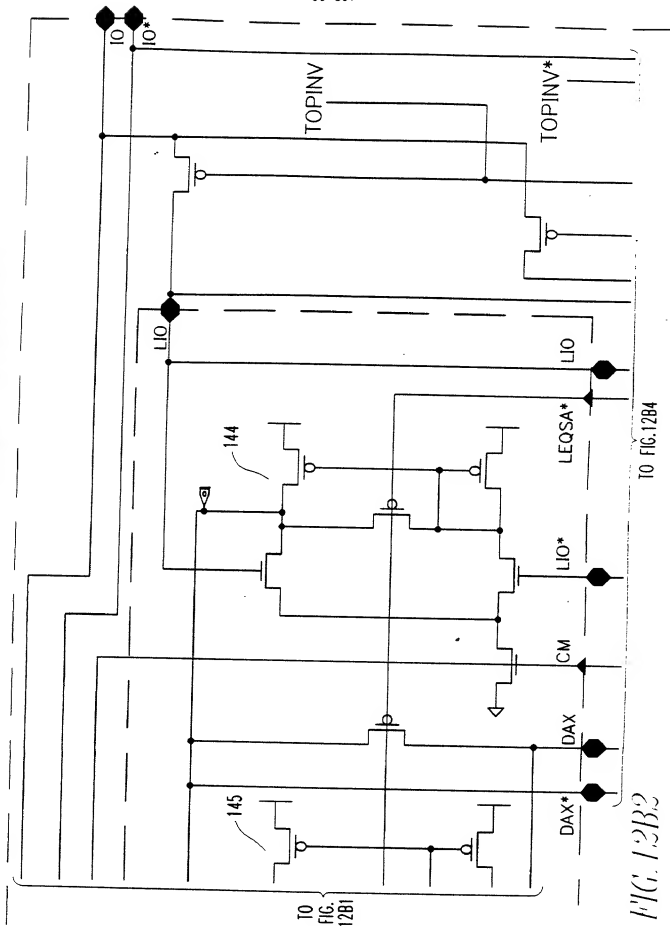
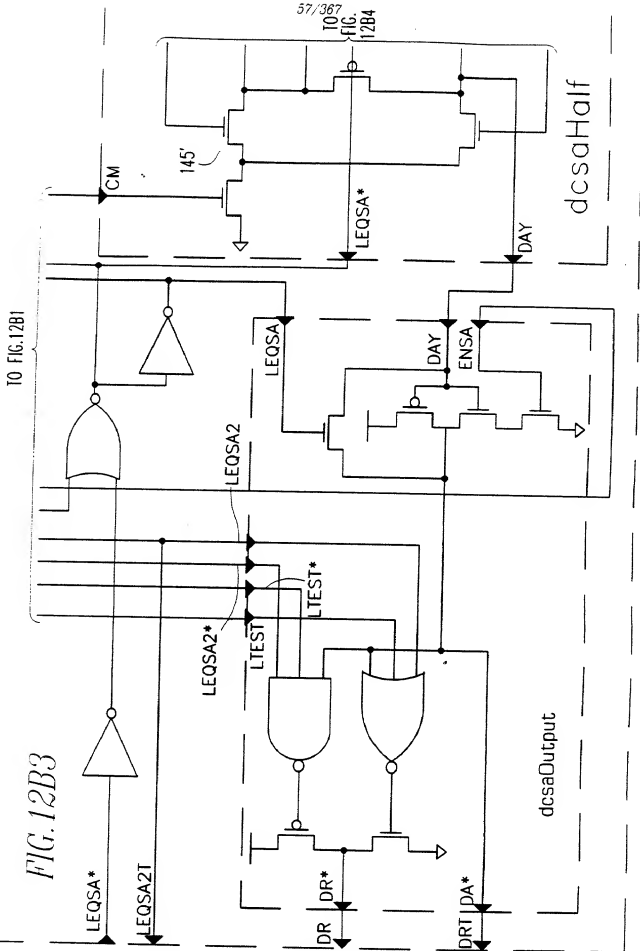


FIG. 12B2

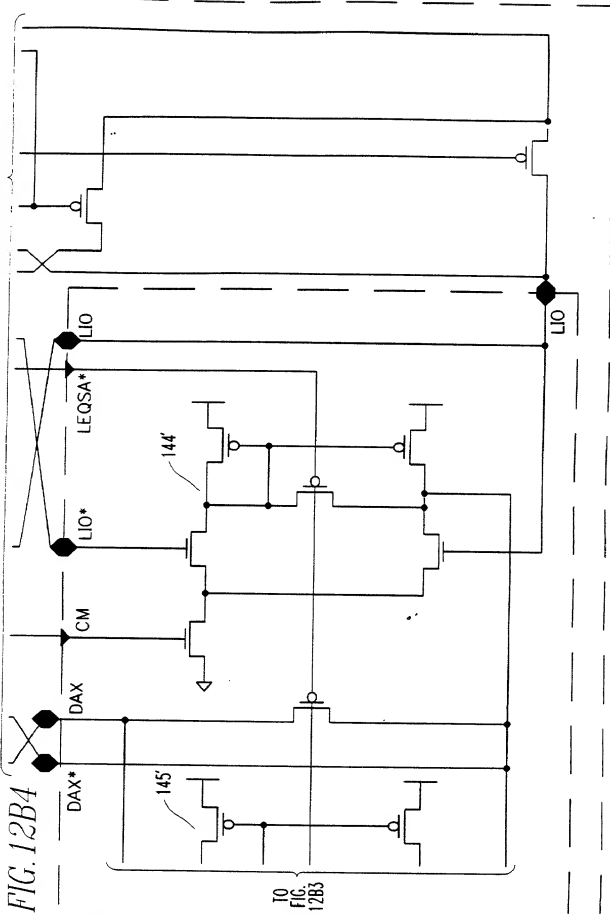
TO FIG. 12B4

FIG. 12B3



IO FIG.12B3

FIG. 12B4



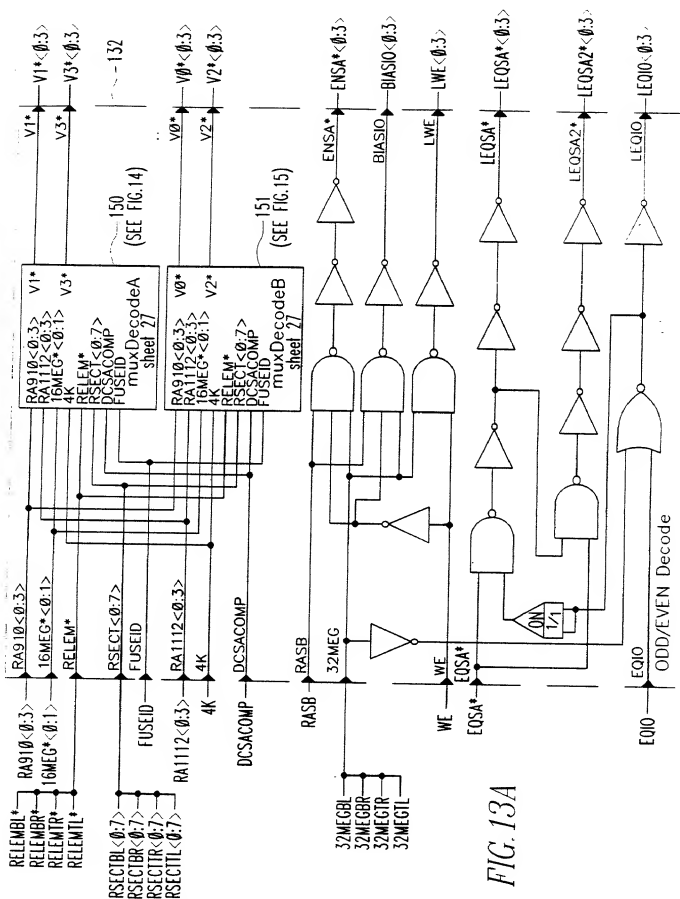
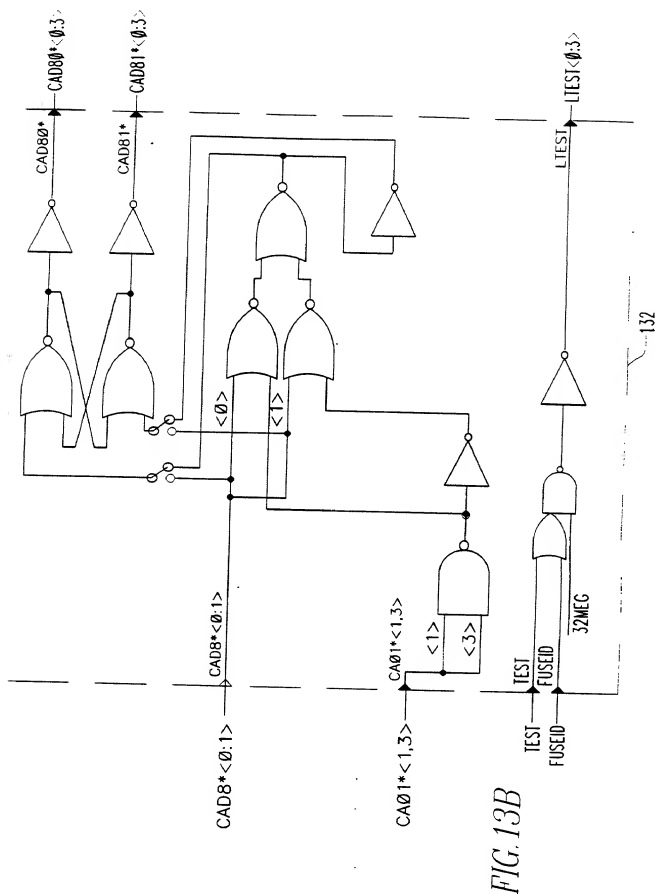


FIG. 13A



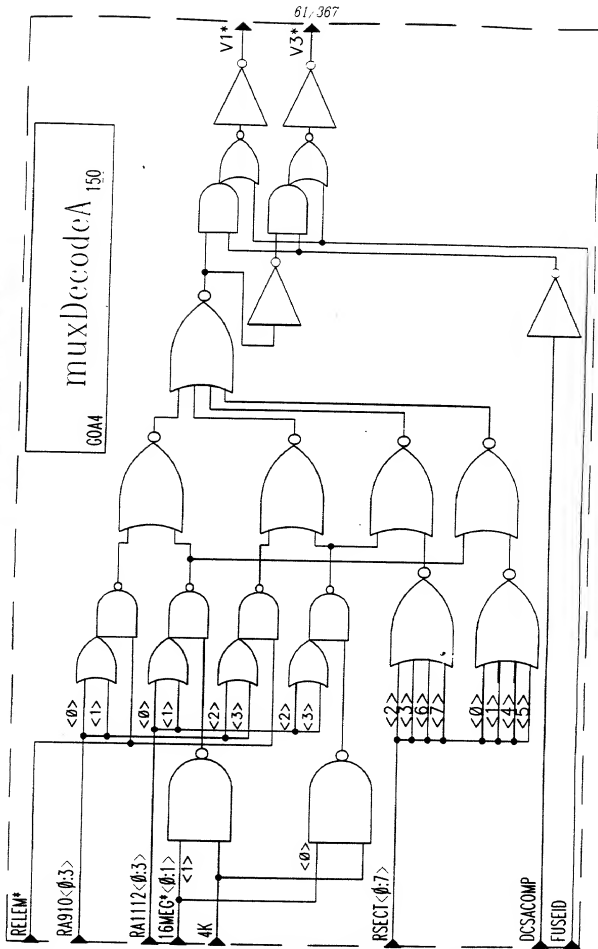


FIG 15-1

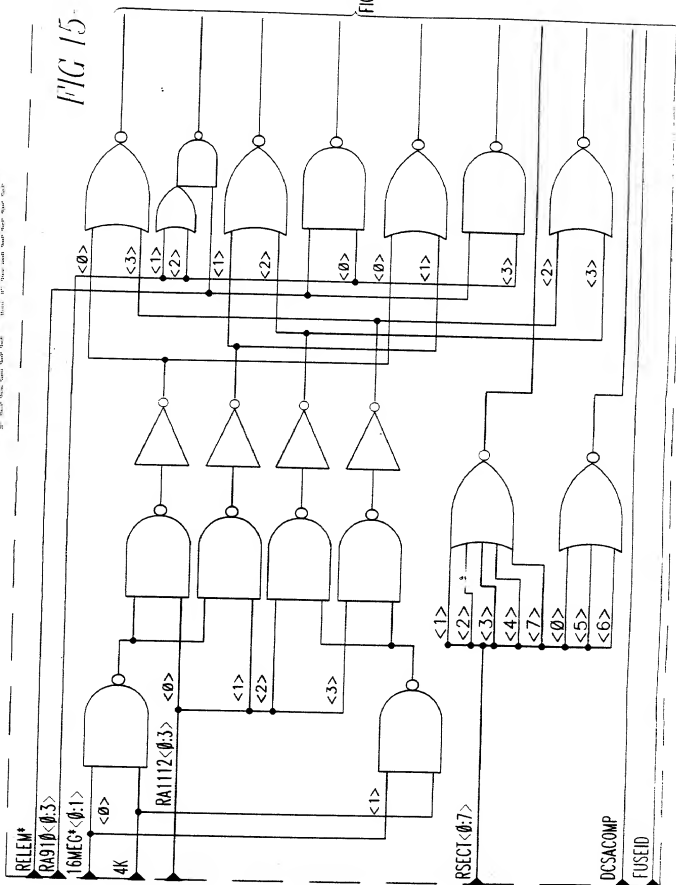


FIG. 15-2

muxDecodeB

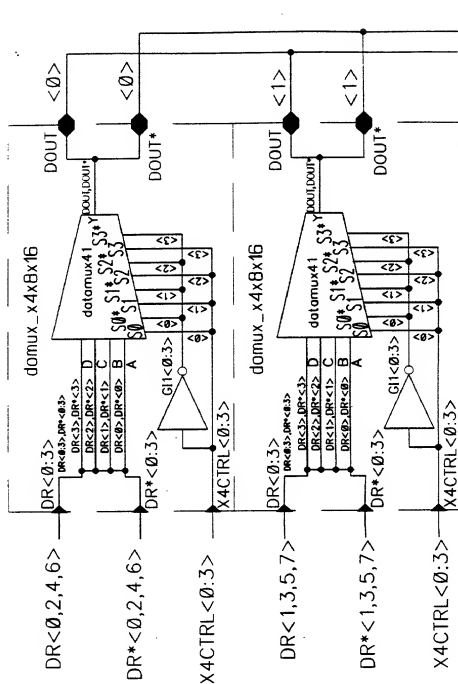
151

V2*1

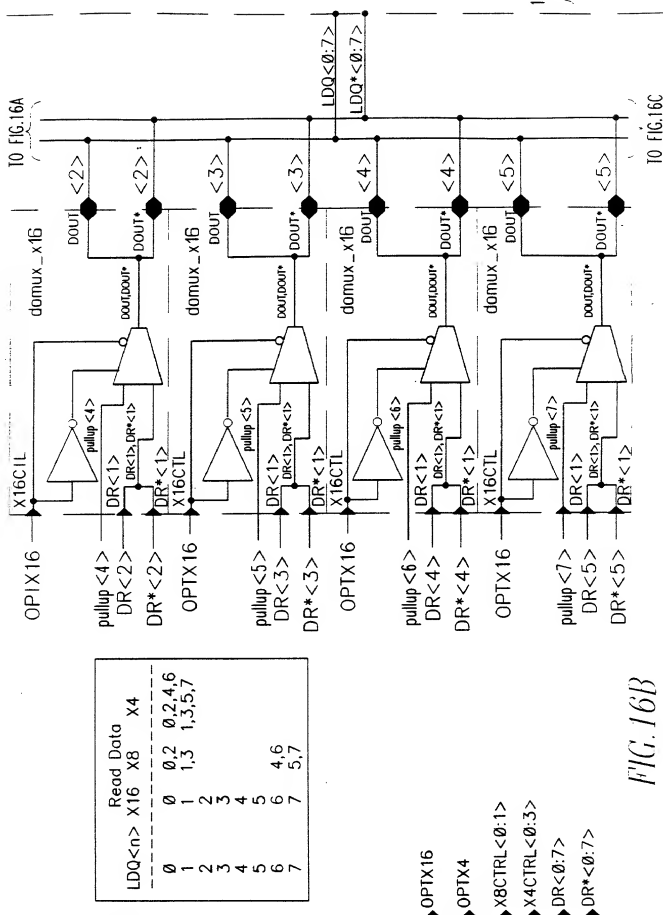
FIG. 15-110

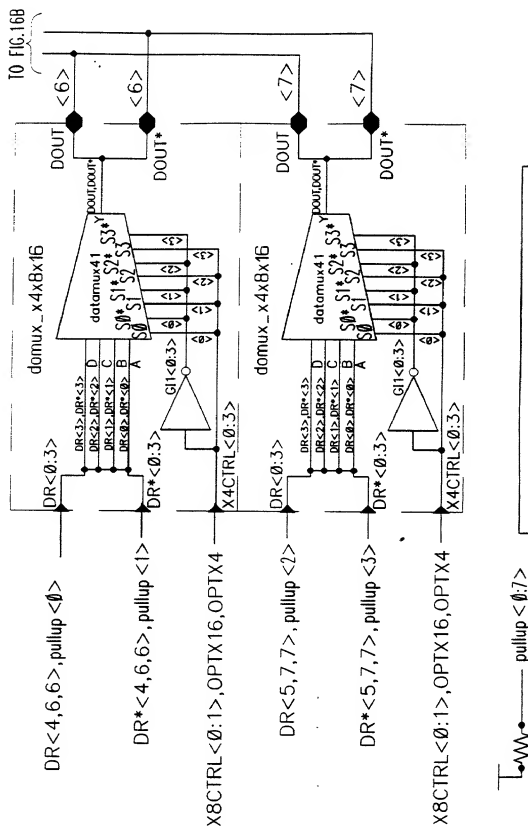
WQ*

FIG. 16A

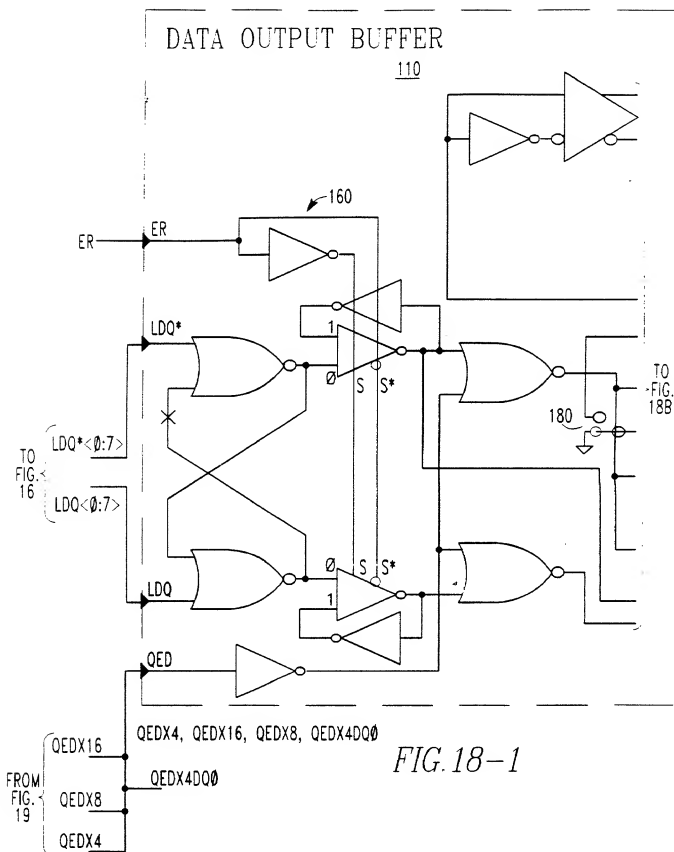


TO FIG. 16B









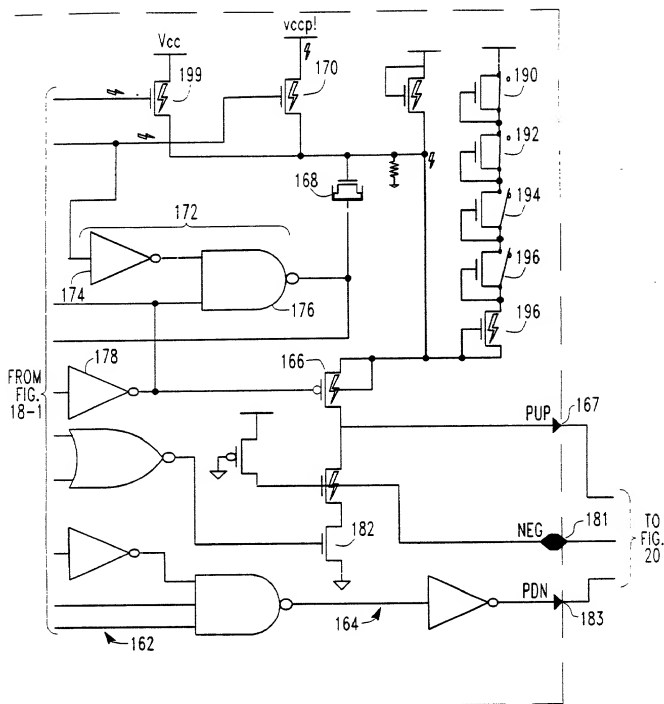
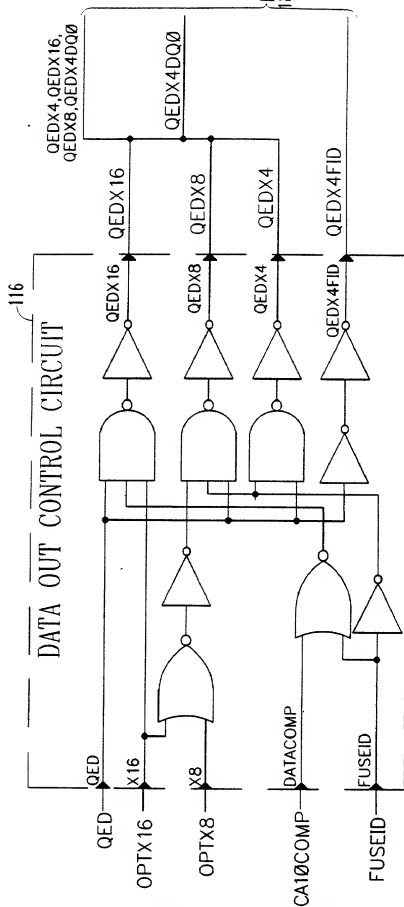


FIG. 18-2



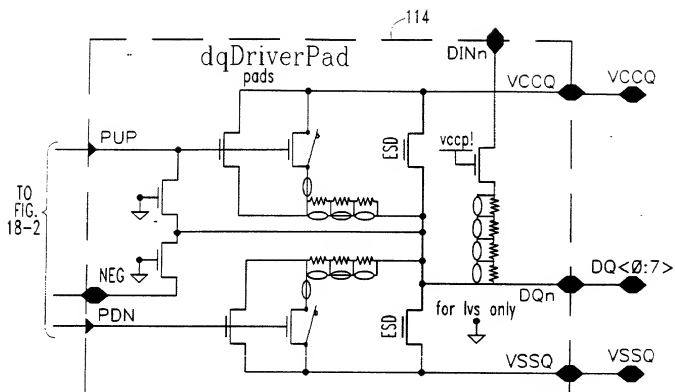


FIG. 20

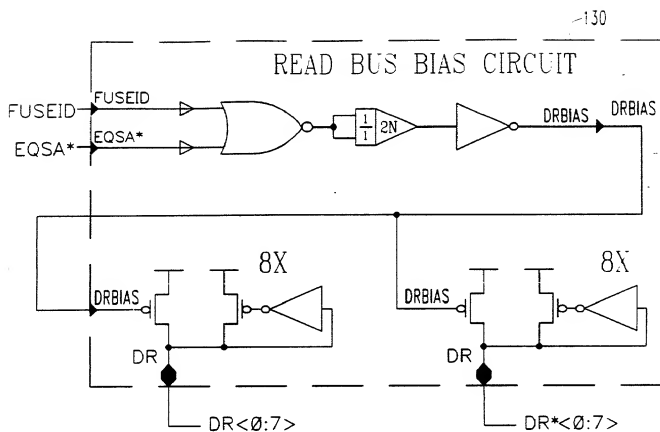
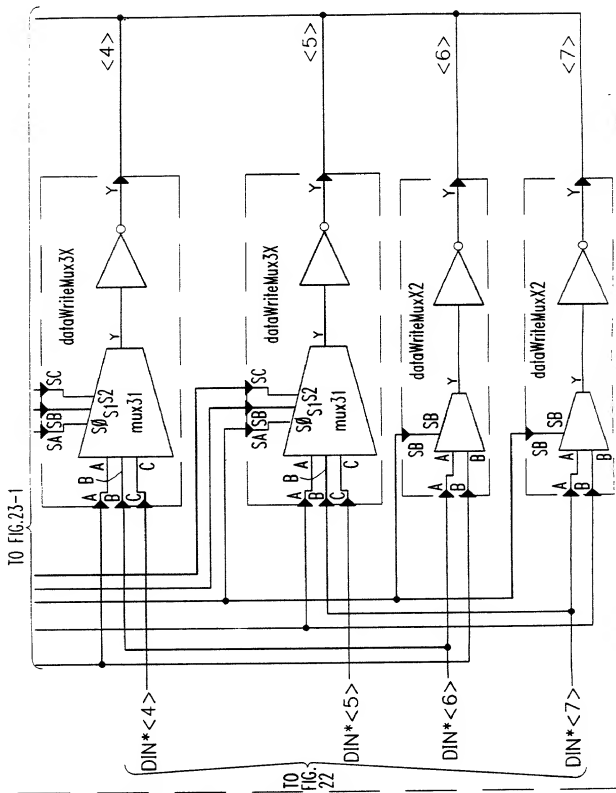


FIG. 21



-122





122

FIG. 23-2

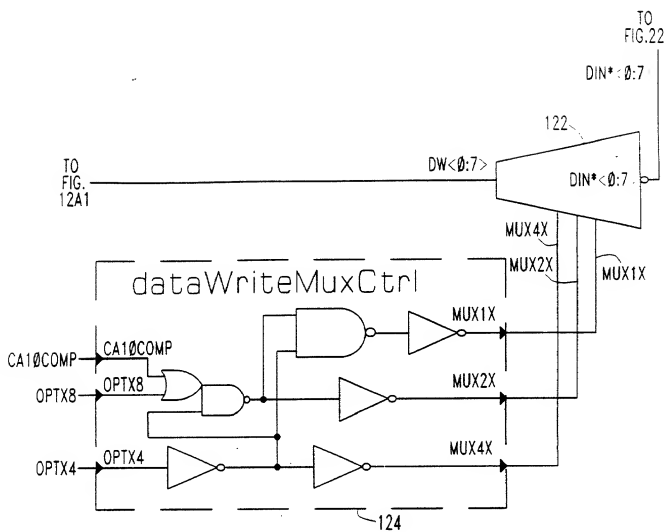


FIG. 24

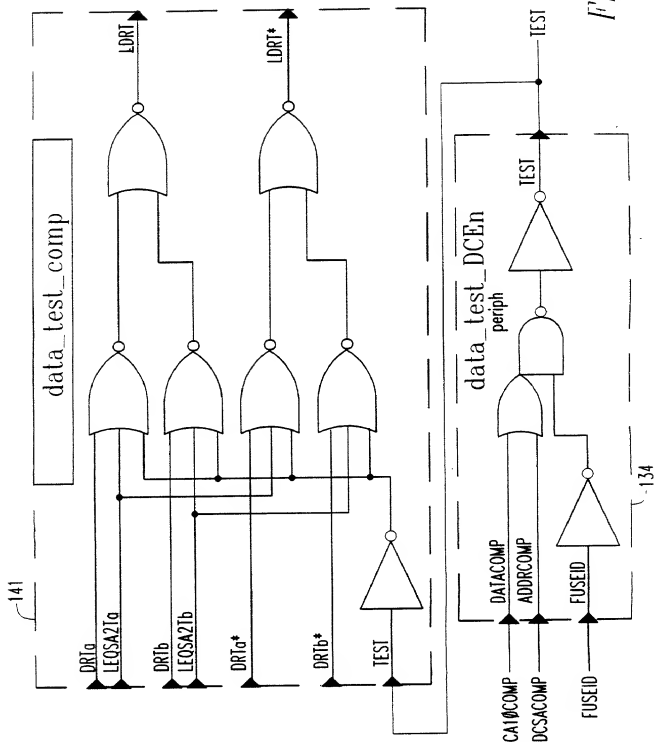
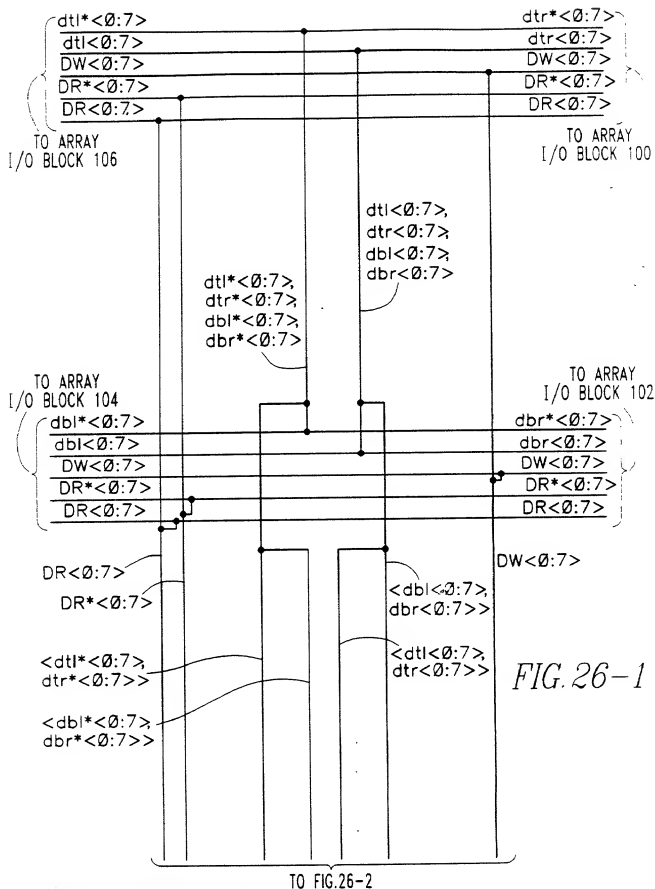


FIG. 25



FROM FIG. 26-1

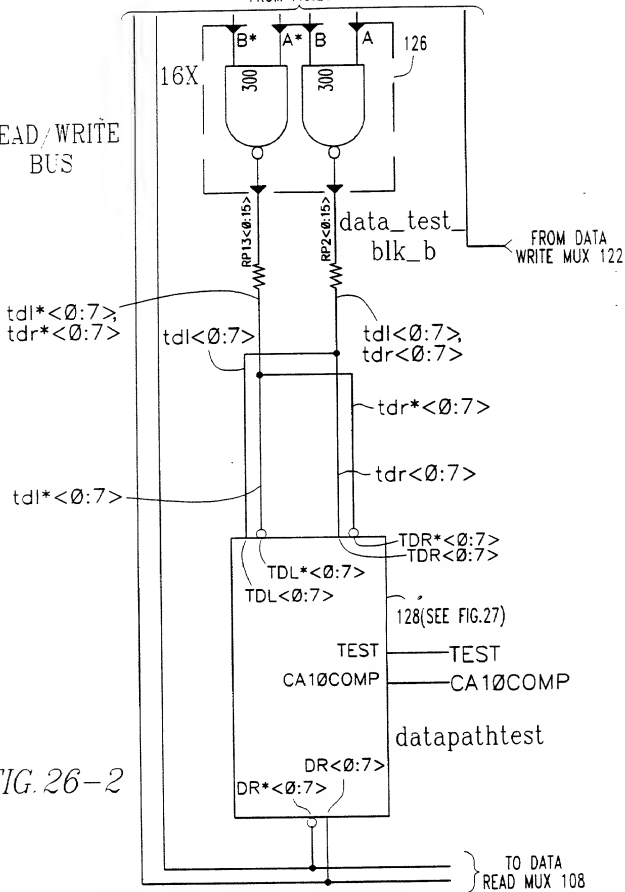
READ/WRITE
BUS

FIG. 26-2

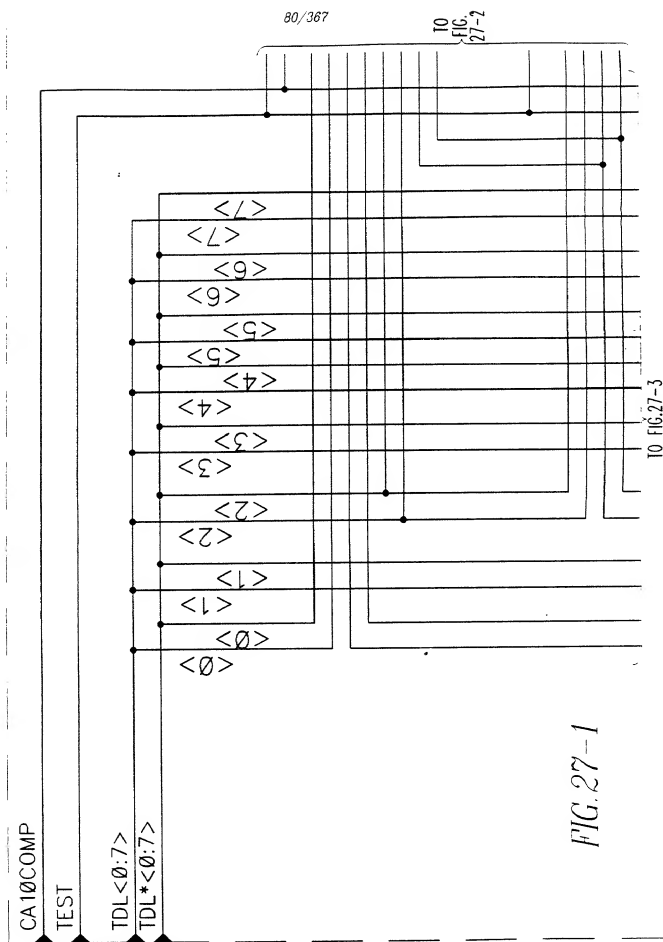
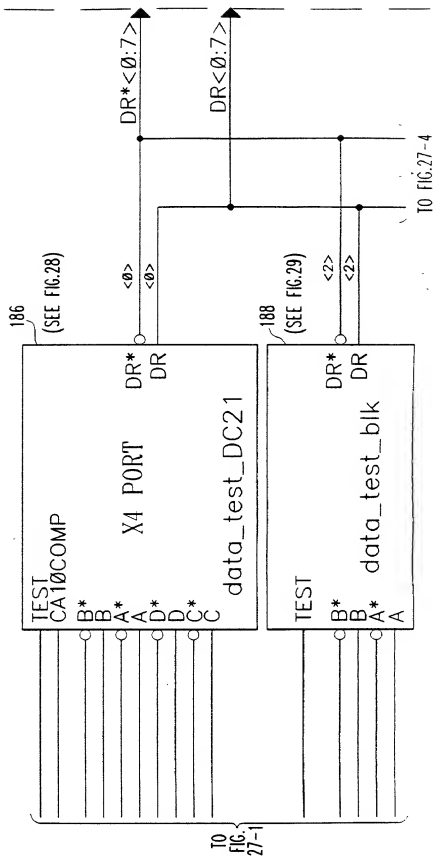


FIG. 27 2

dataPathTest
Block

128



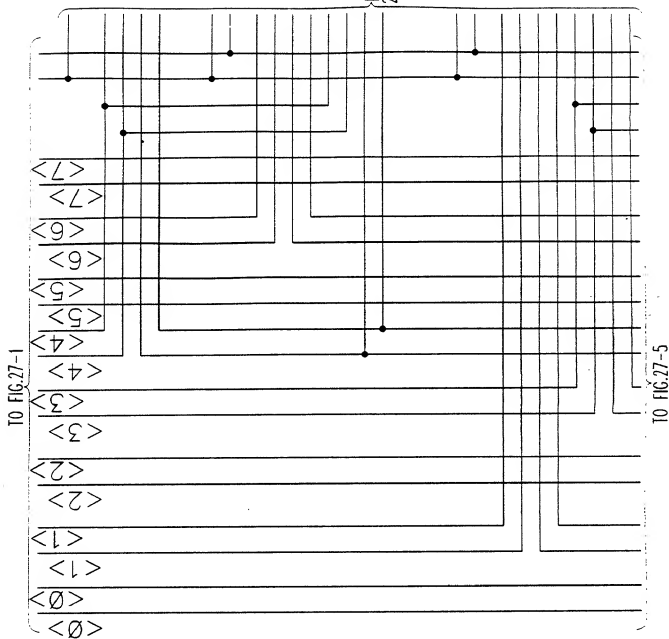
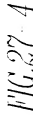
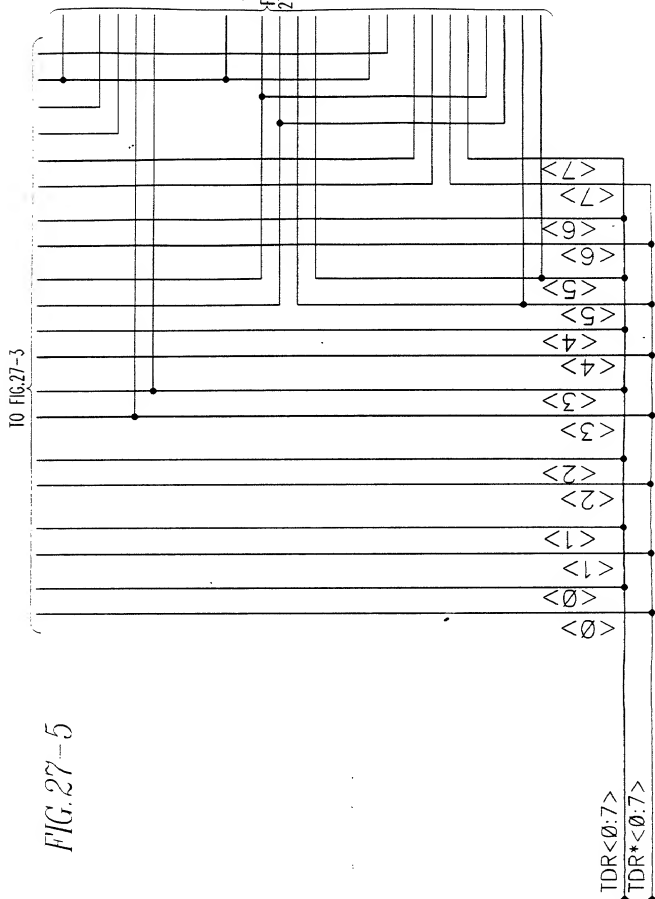
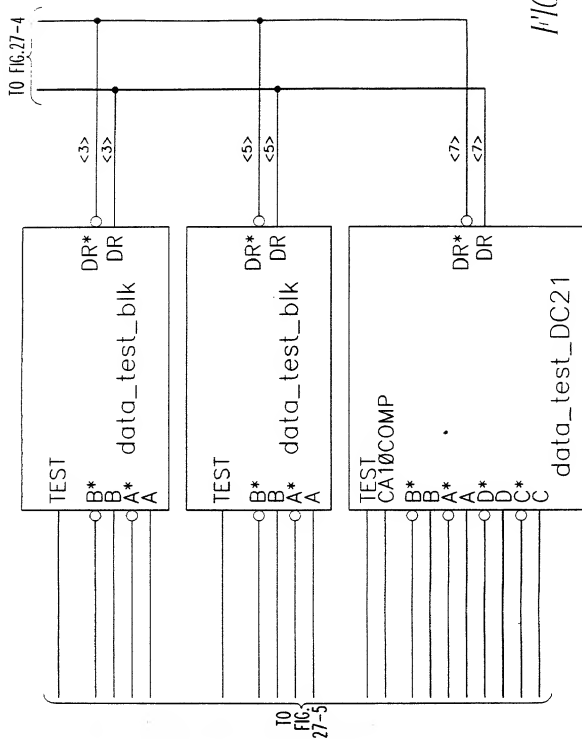


FIG. 27-3







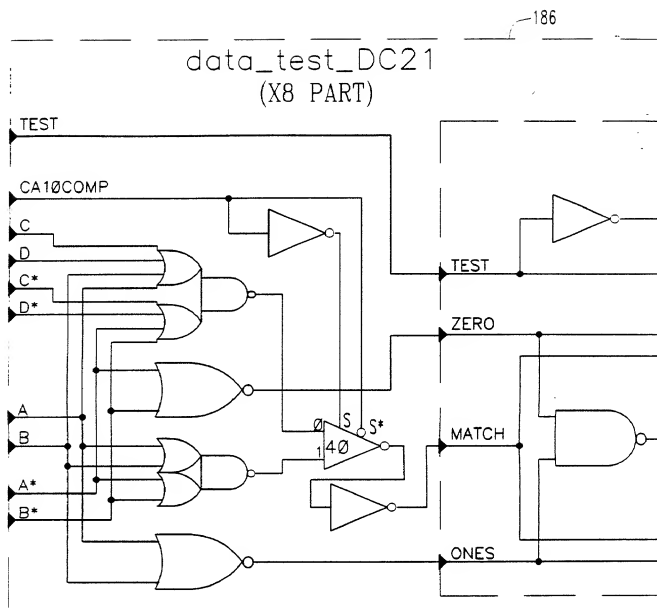


FIG. 28-1

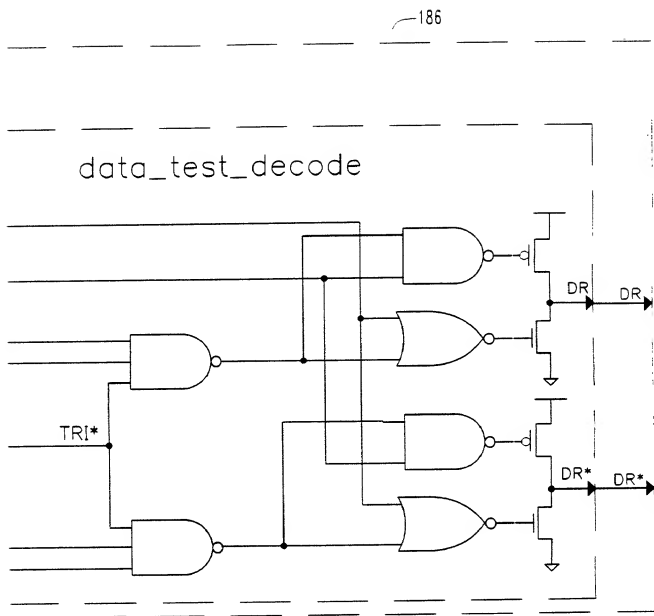


FIG. 28-2

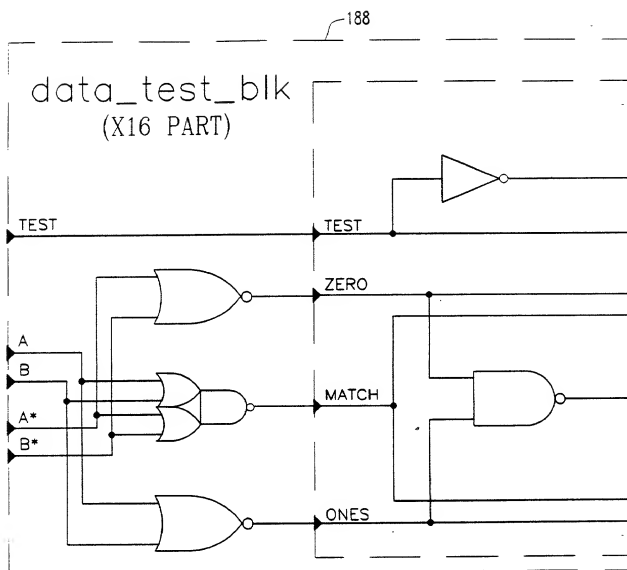


FIG. 29-1

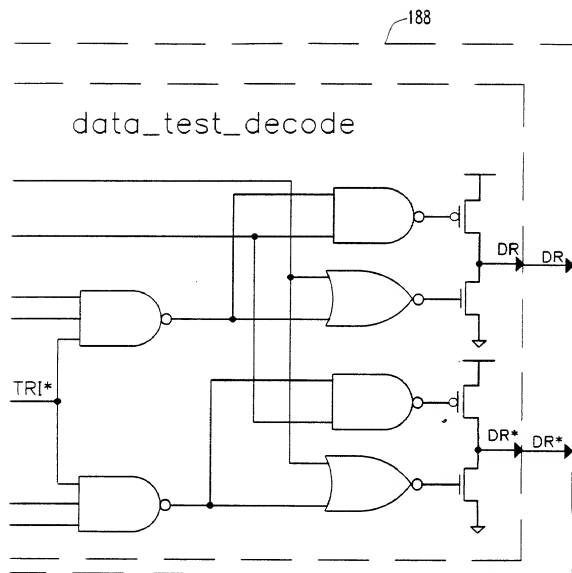
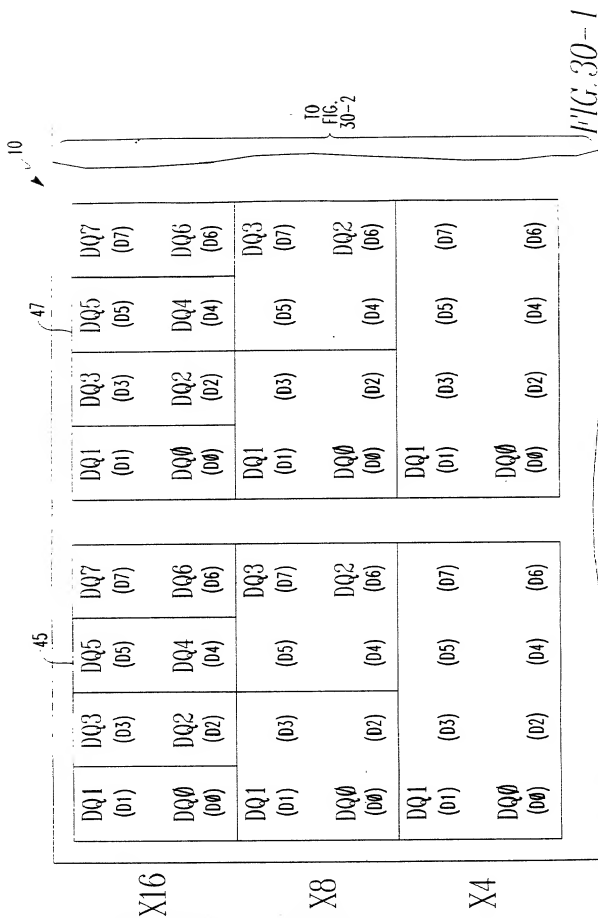
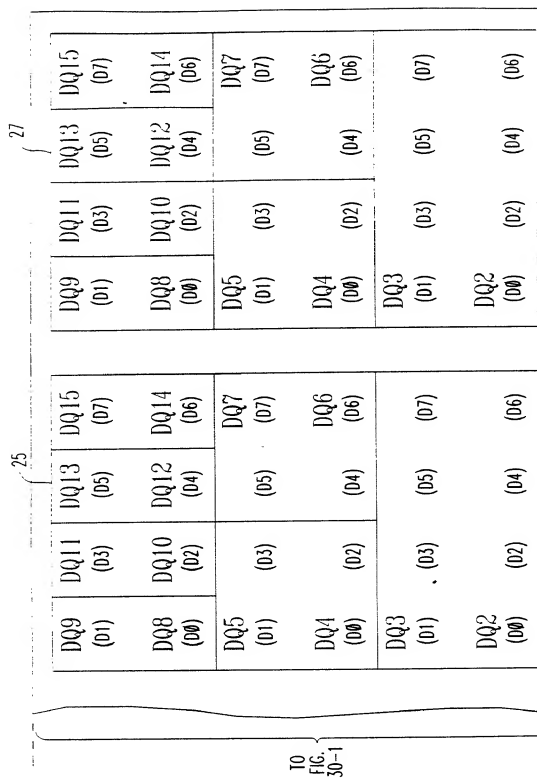


FIG. 29-2



TO FIG. 30-3



10 FIG. 30-4

TO FIG. 30-1

38		(00) DQ0	(02)	(04)	(06)
		(01) DQ1	(03)	(05)	(07)
40		(00) DQ0	(02)	(04)	(06)
		(01) DQ1	(03)	(05)	(07)
10 FIG. 30-4		(00) DQ0	(02)	(04)	(06) DQ2
		(01) DQ1	(03)	(05)	(07) DQ3
		(00) DQ0	(02) DQ2	(04) DQ4	(06) DQ6
		(01) DQ1	(03) DQ3	(05) DQ5	(07) DQ7

X4

X8

X16

FIG. 30-3

10 FIG. 30-2

33		
(00) DQ2	(02)	(04) (06)
(01) DQ3	(03)	(05) (07)
(00) DQ4	(02)	(04) (06) DQ6
(01) DQ5	(03)	(05) (07) DQ7
(00) DQ8	(02) DQ10	(04) DQ12 (06) DQ14
(01) DQ9	(03) DQ11	(05) DQ13 (07) DQ15

10
FIG.
30-3

31		
(00) DQ2	(02)	(04) (06)
(01) DQ3	(03)	(05) (07)
(00) DQ4	(02)	(04) (06) DQ6
(01) DQ5	(03)	(05) (07) DQ7
(00) DQ8	(02) DQ10	(04) DQ12 (06) DQ14
(01) DQ9	(03) DQ11	(05) DQ13 (07) DQ15

FIG. 30-1

X4		VSSQ	N/C	VSSQ	N/C	N/C	
X8		VSSQ	DQ3	VSSQ	DQ2	N/C	
X16		VSSQ	DQ7	VSSQ	DQ6	DQ5	
	1	2	3	4	5	6	7
							8
							9
							10
							11
X16	VCCQ	DQ0	DQ1	VCCQ	DQ1	DQ2	VCCQ
X8	VCCQ	DQ0	DQ1	VCCQ	DQ1	N/C	N/C
X4	VCCQ	DQ0	DQ1	VCCQ	DQ1	N/C	N/C

TO FIG. 31A2

FIG. 31A1

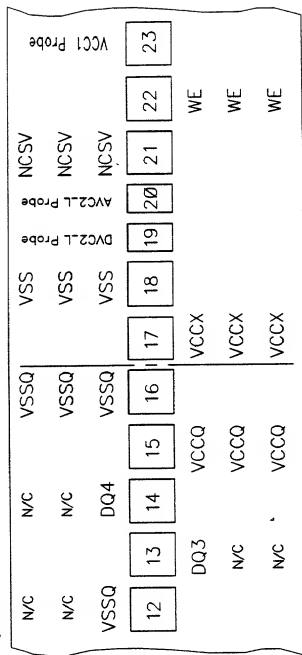
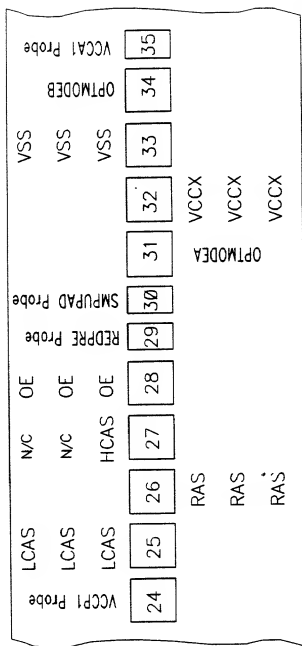


FIG. 31A2



TO FIG. 3182

FIG. 31B1

TO FIG. 31B1

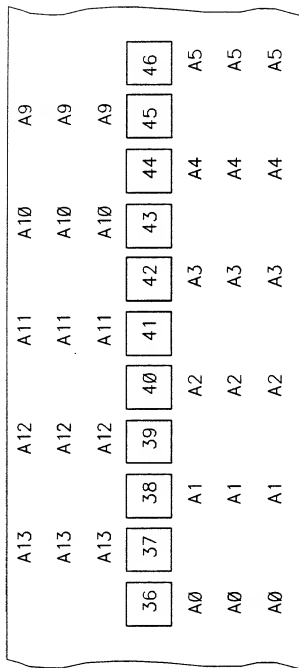


FIG. 31B2

A8	47	A7	VSS	VSSQ	N/C
A8	48	A7	VSS	VSSQ	DQ7
A8	49	A7	VSS	VSSQ	DQ15
	50	TTL SV			
	51	DVC2_R Probe	54	55	56
	52	AVC2_R Probe	53		57
			VCCX	VCCQ	DQ8
A6			VCCX	VCCQ	DQ4
A6			VCCX	VCCQ	DQ2
					N/C
					N/C

TO FIG. 31C2

FIG. 31C1

[illegible]

FIG. 31C2

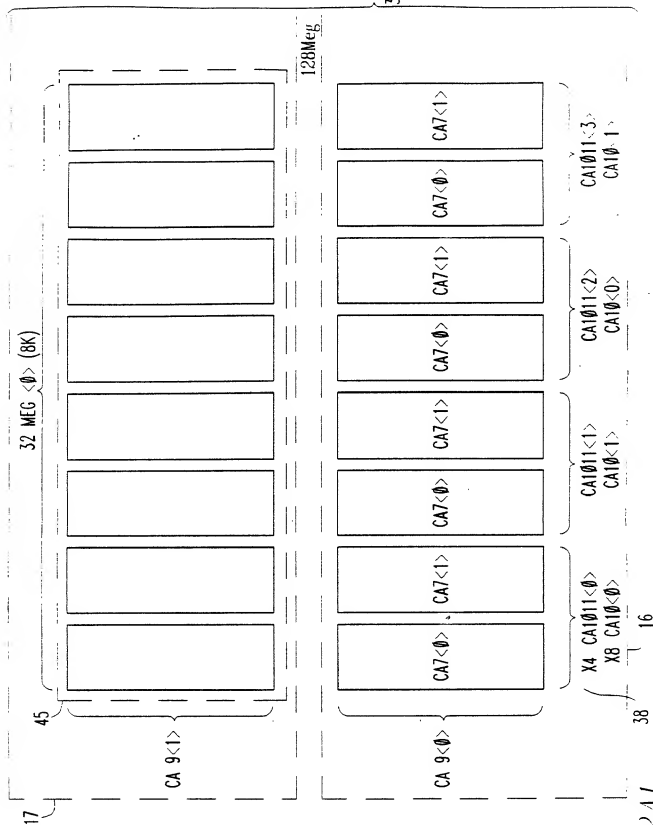


FIG. 32A1

PART TYPE	32MEG
ANY 16K	RA 13
X4 8K OR 4K	CA 12
X8 8K OR 4K	CA 11
X16 8K OR 4K	CA 10

FIG. 32A2

CA 6<0:1> MSB
 CA45<0:3>
 CA23<0:3>
 CA01<0:3>
 CA 8<0:1> LSB

32 MEG <1> (8K)

47

LSB → MSB

40

FROM
FIG.
32A1

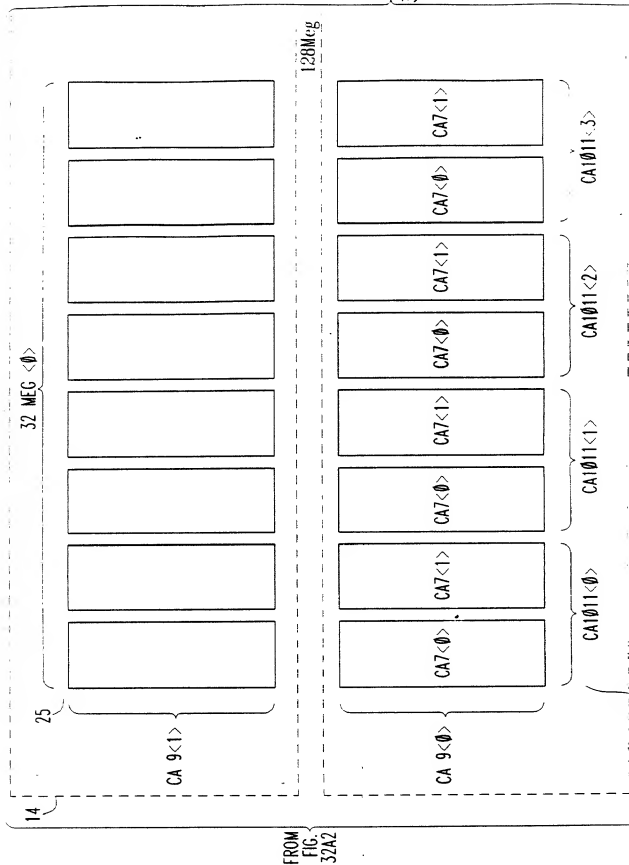
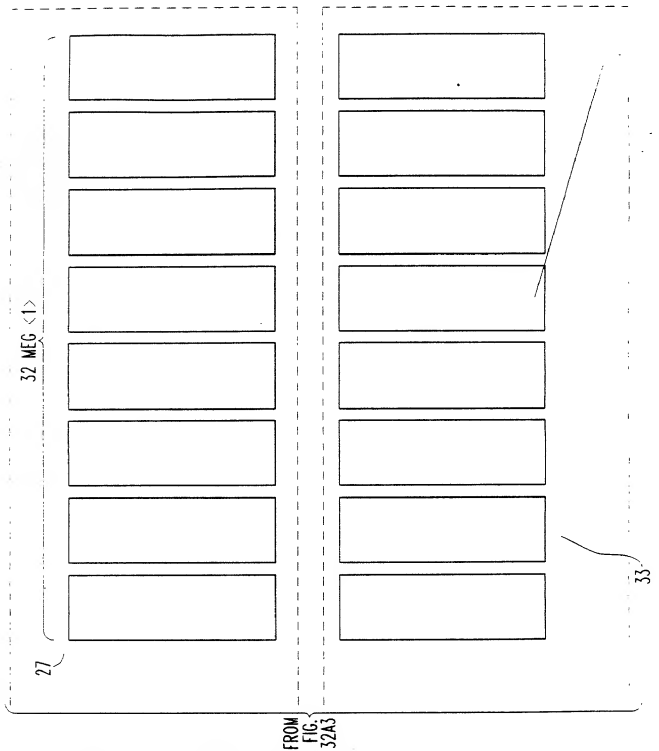


FIG. 32A4



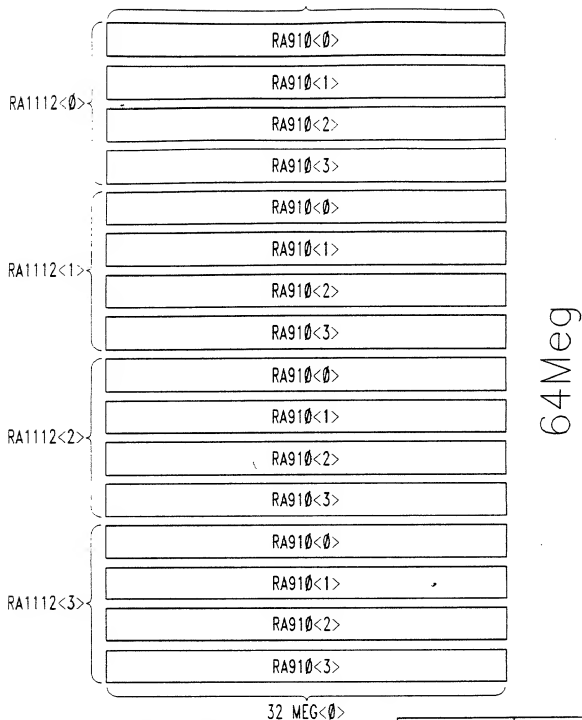


FIG. 32B1

PART TYPE	32MEG
ANY 16K	RA_13
X4 8K OR 4K	CA_12
X8 8K OR 4K	CA_11
X16 8K OR 4K	CA_10

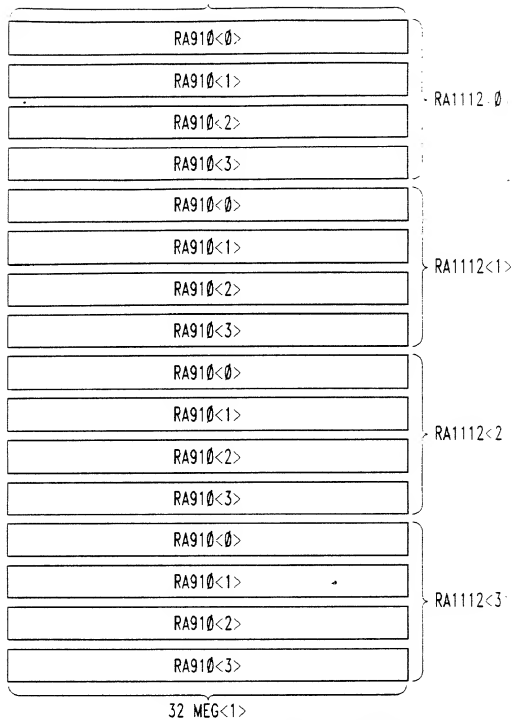
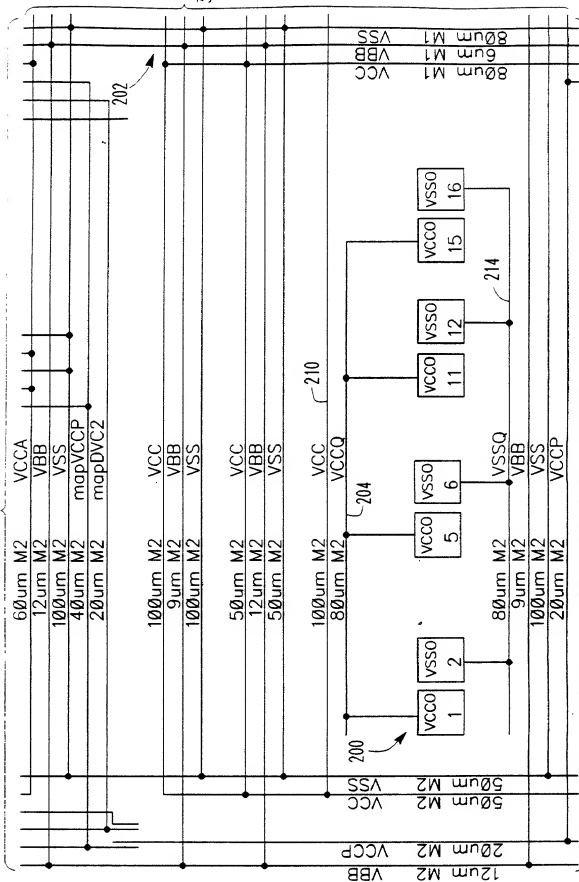


FIG. 32B2

FROM FIG. 33A1



TO
FIG.
33B3

107/367

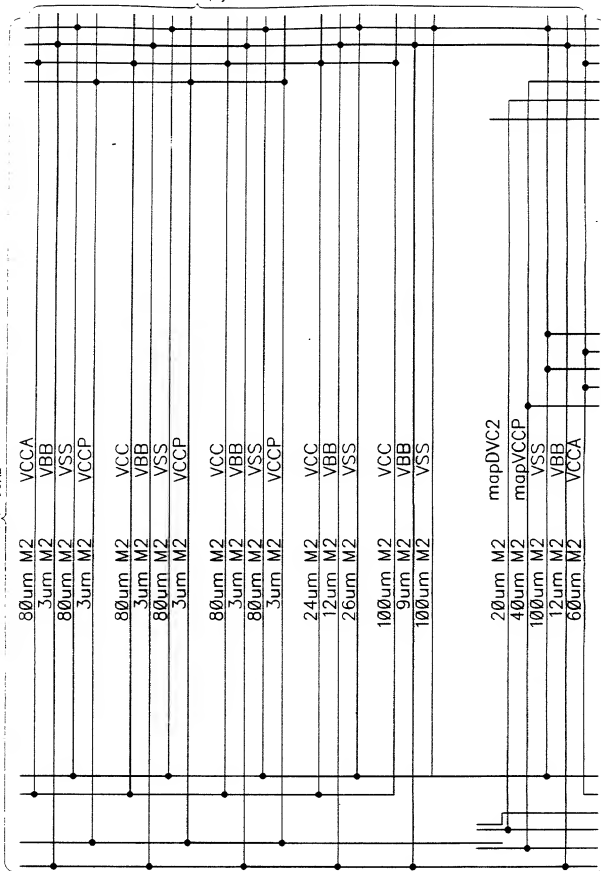
TO FIG. 33A3

FIG. 33A2

TO
FIG.
3385

108, 367

FROM FIG. 33A2

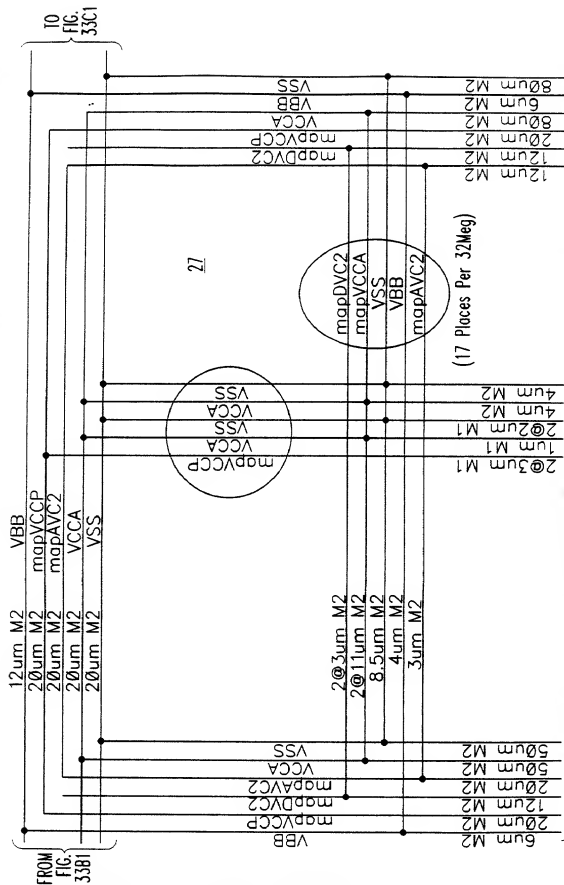


TO FIG. 33A4

FIG. 33A3



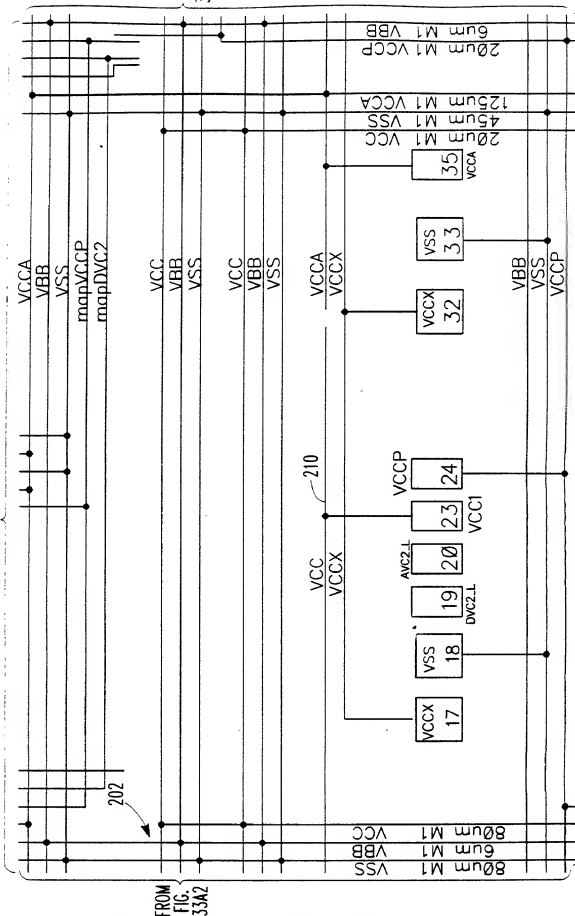
1463331



TO FIG. 3384

FIG. 33B2

FROM FIG. 33B1



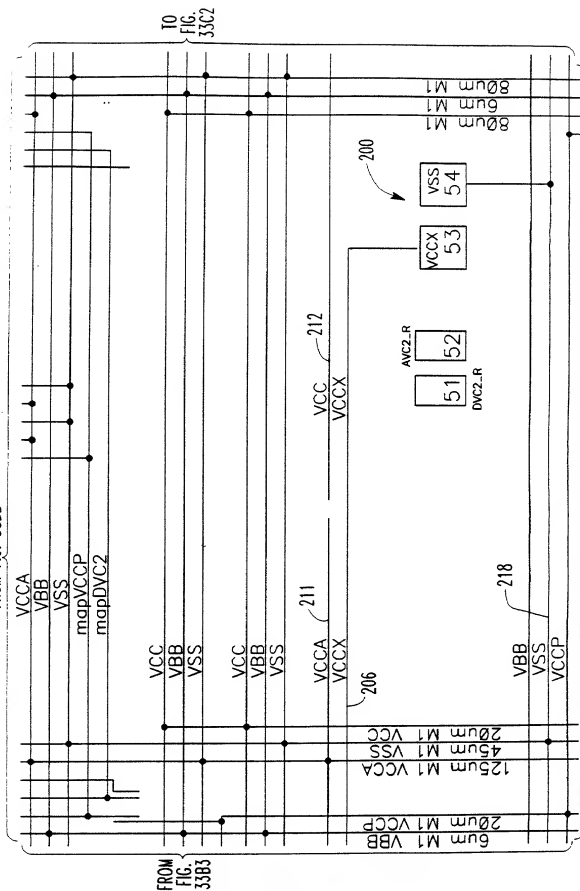
TO FIG. 33B3

FIG. 33B3

TO
FIG.
33B4

112/367

FROM FIG. 33B2

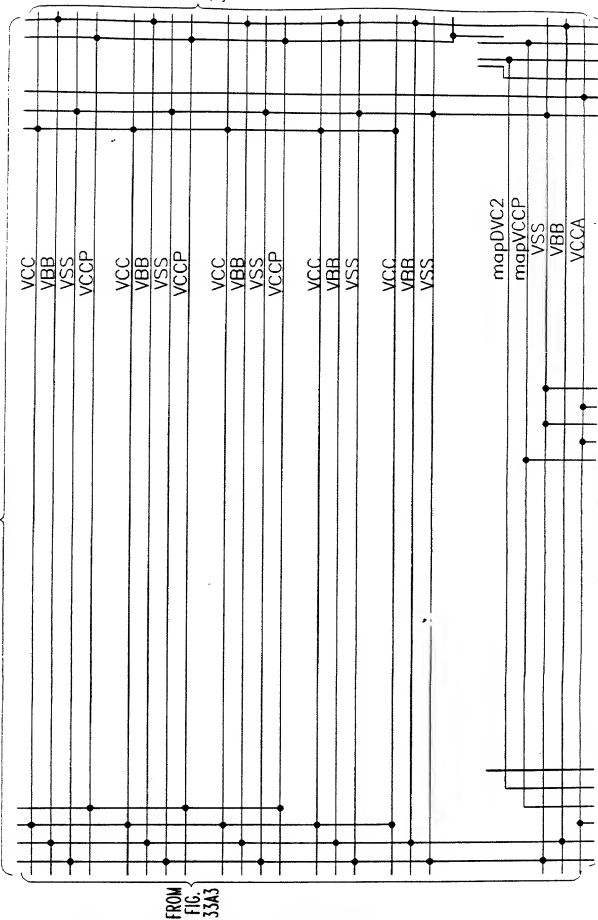


TO FIG. 33B6

FIG. 33B1

114/367

FROM FIG. 33B3



TO FIG. 33B7

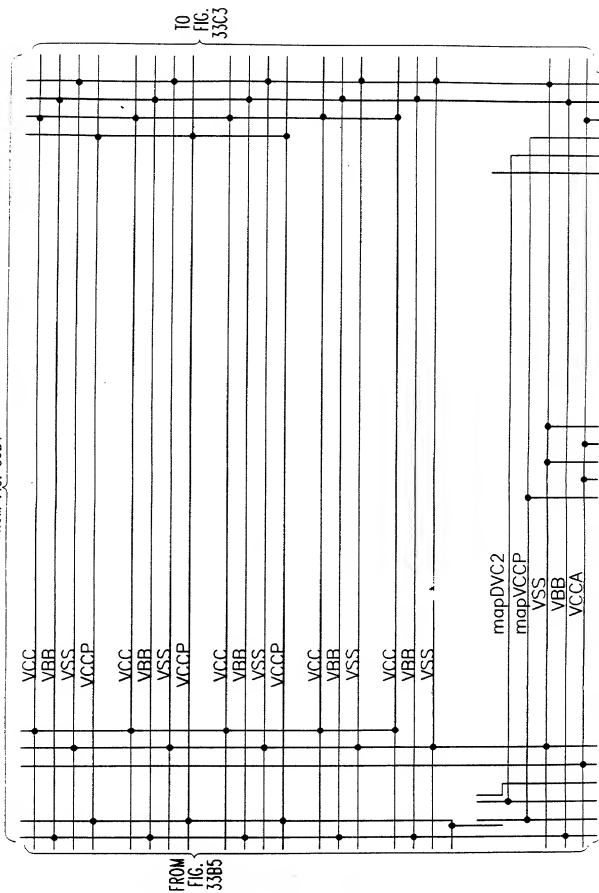
FIG. 33B5

FROM
FIG.
33A3

TO
FIG.
33B6

114/367

FROM FIG. 33B4



TO FIG. 33B8

FIG. 33B6

FROM
FIG.
33A4

TO
FIG.
3388

296337

FROM FIG. 3386

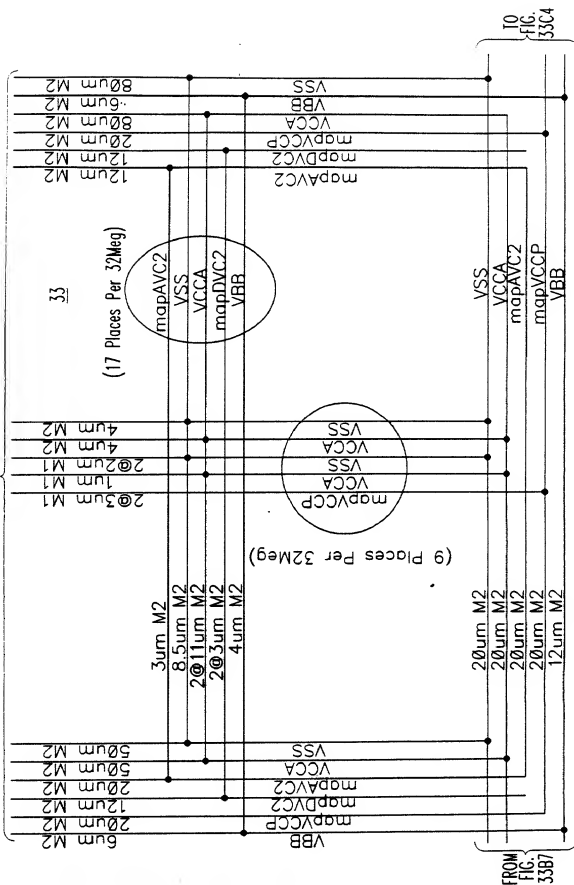
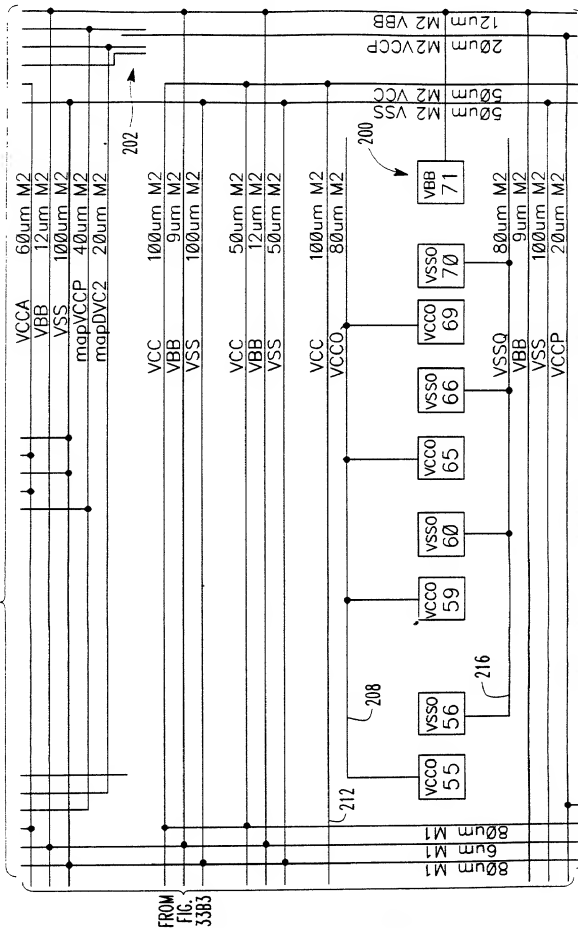




FIG. 33C1

FROM FIG. 33C1

FROM
FIG.
33B3

TO FIG. 33C3

FIG. 33C2

FROM FIG. 33C2

FROM
FIG.
33B6

TO FIG. 33C4

17/6/33

FROM FIG. 33C3

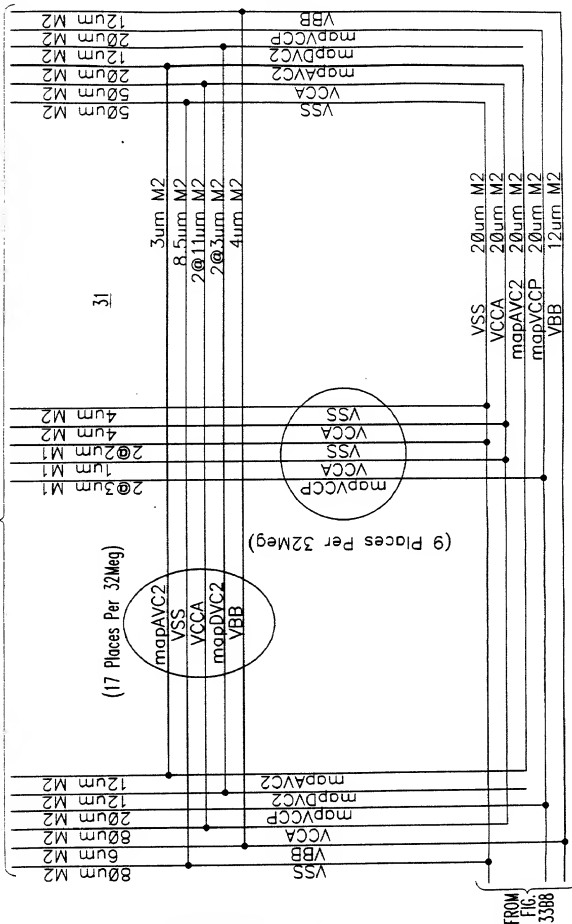
FROM
FIG.
33B8

FIG. 33C4

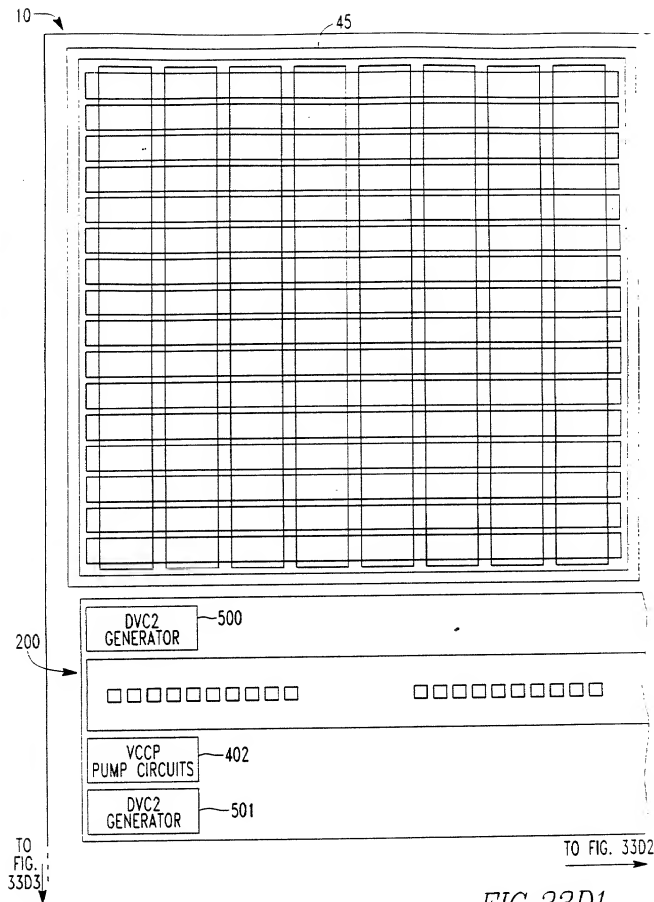
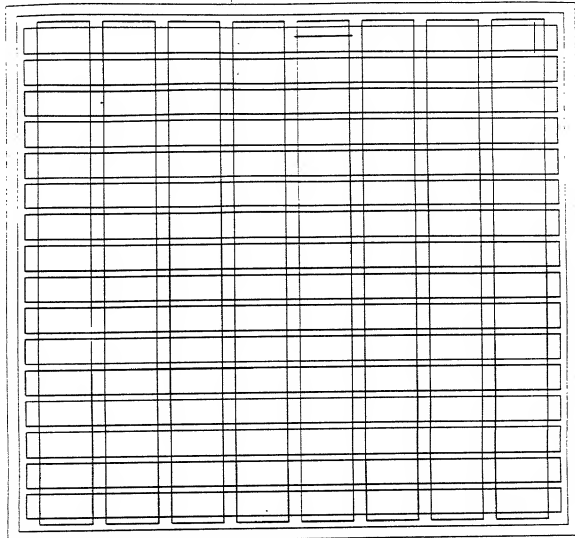


FIG. 33D1

TO FIG. 33D1

47



502

DVC2
GENERATOR

401

VCCP
PUMP CONTROL

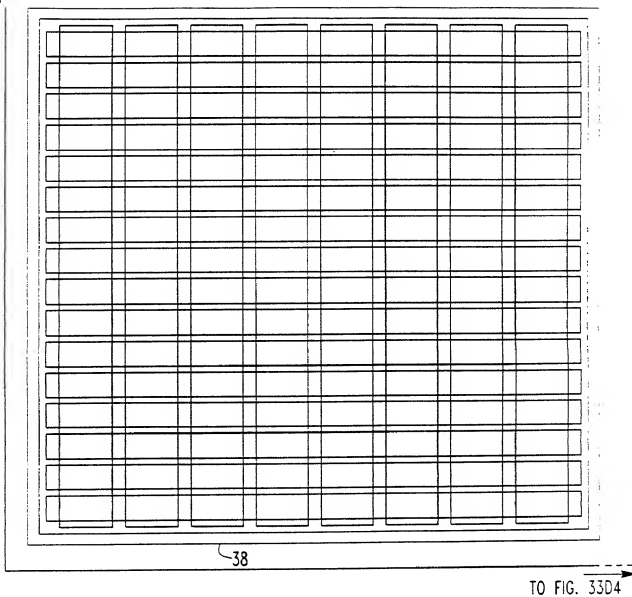
503

DVC2
GENERATORTO
FIG.
33D4

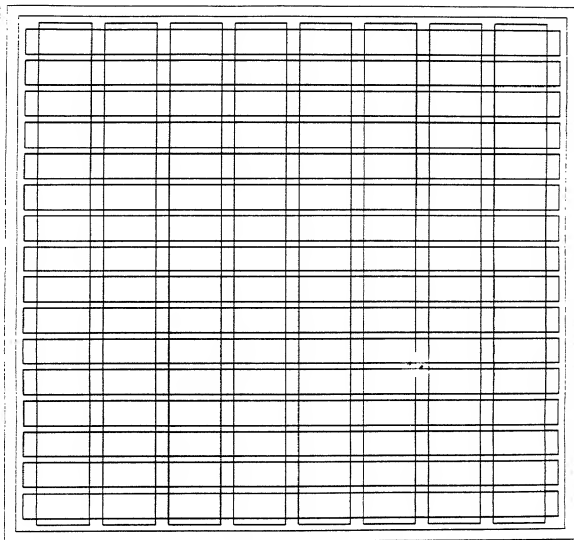
FIG. 33D2

TO
FIG.
33D1

(SEE FIG. 33E1)

*FIG. 33D3*

TO
FIG.
33D2



40

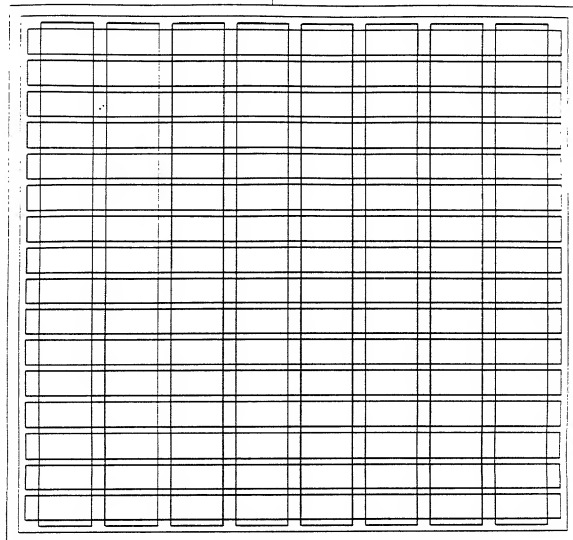
TO FIG. 33D3

FIG. 33D4

(SEE FIG. 33D2)

25

TO FIG. 33E2



DVC2
GENERATOR 504

□ □ □ □ □ □ □ □

□ □ □ □ □ □ □ □

VCCP
REGULATOR 220

DVC2
GENERATOR 505

TO
FIG.
33E3

FIG. 33E1

127/367

TO FIG. 33E1

27

10

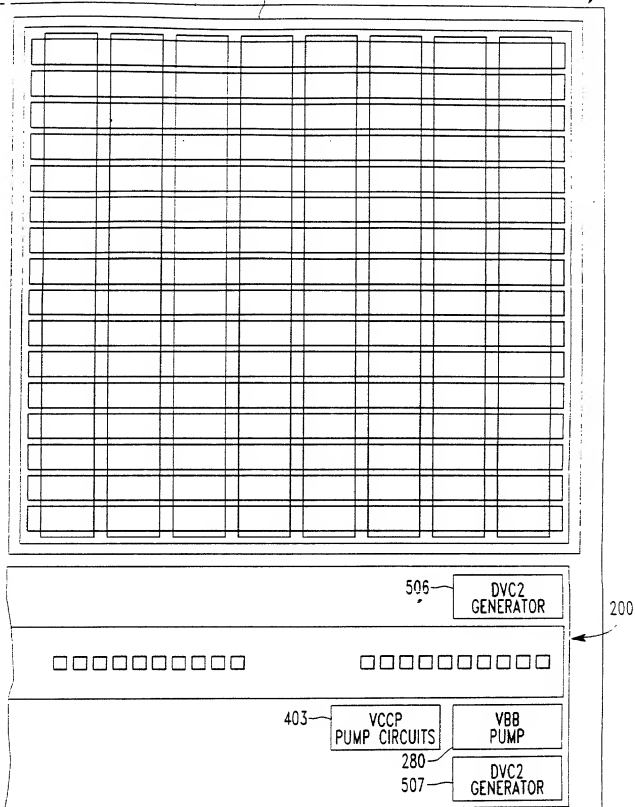


FIG. 33E2

TO
FIG.
33E4

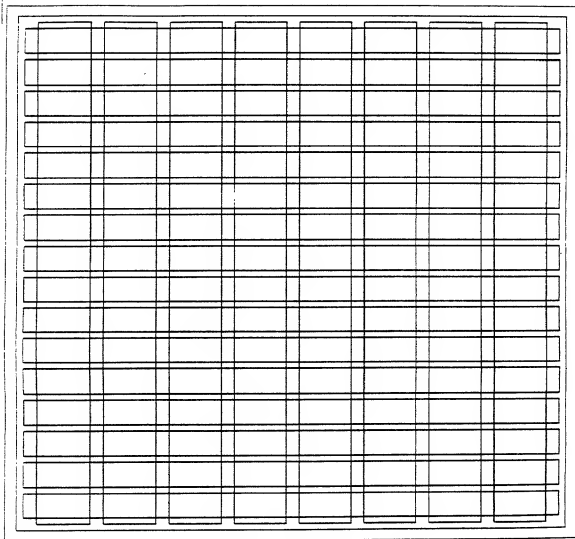
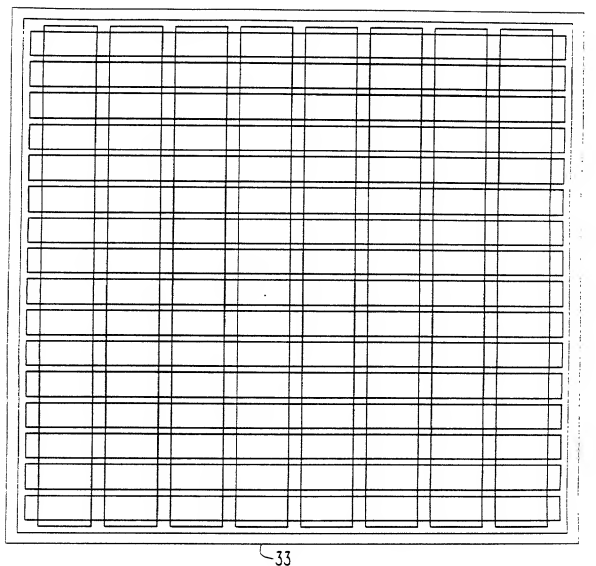
TO
FIG.
33E1

FIG. 33E3

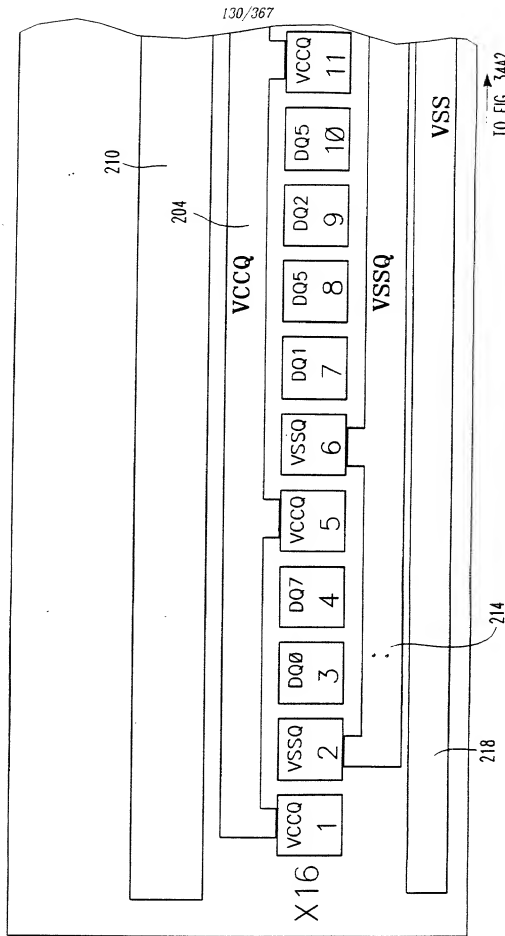
TO FIG. 33E4



TO
FIG.
33E2

TO FIG. 33E3

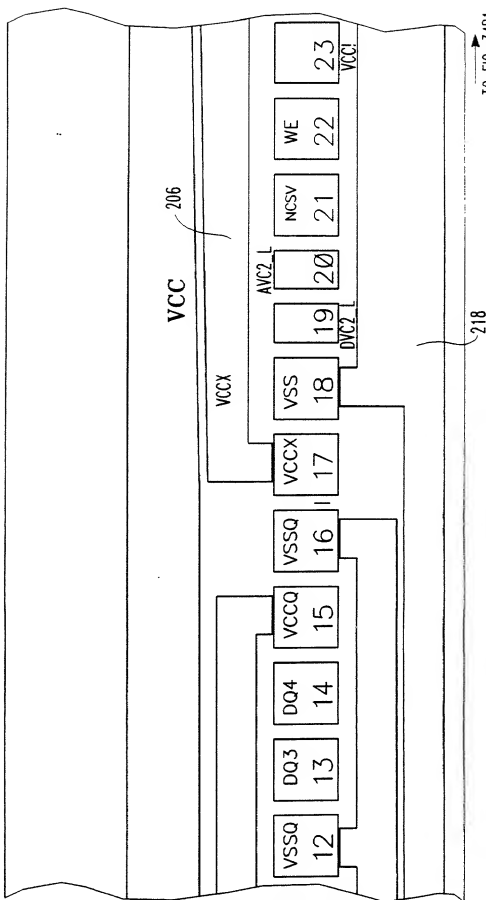
FIG. 33E4



TO FIG. 34A2

FIG. 34A1

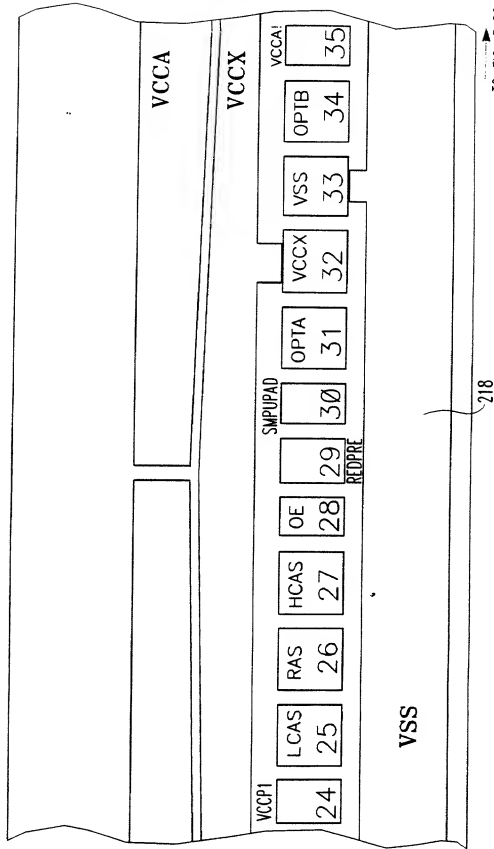
TO FIG. 34A1



TO FIG. 34B1

FIG. 34A2

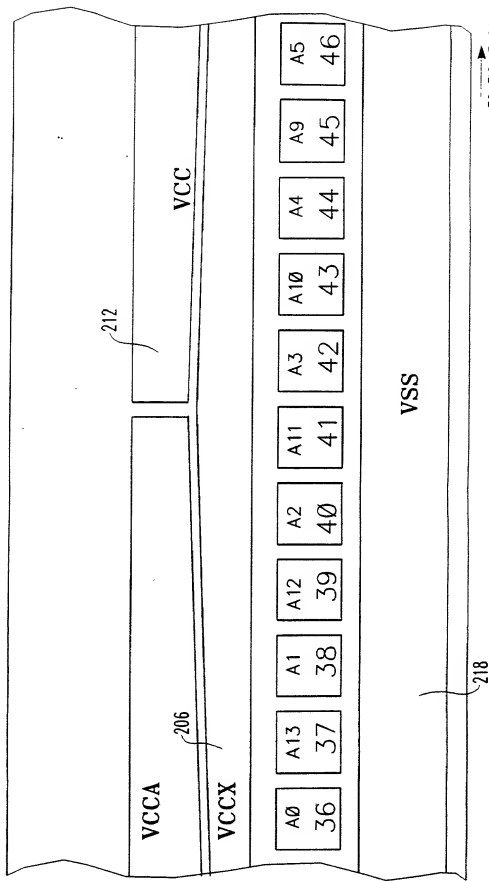
TO FIG. 34A2



TO FIG. 34B2

FIG. 34B1

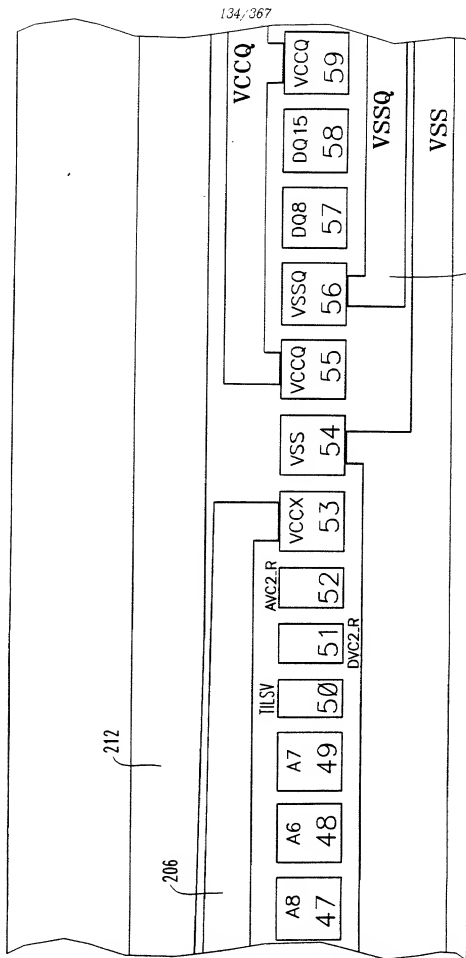
TO FIG. 34B1



TO FIG. 34C1

FIG. 34B2

TO FIG. 34B2



TO FIG. 34C2

FIG. 34C1

FIG. 34C2

TO FIG. 34C1

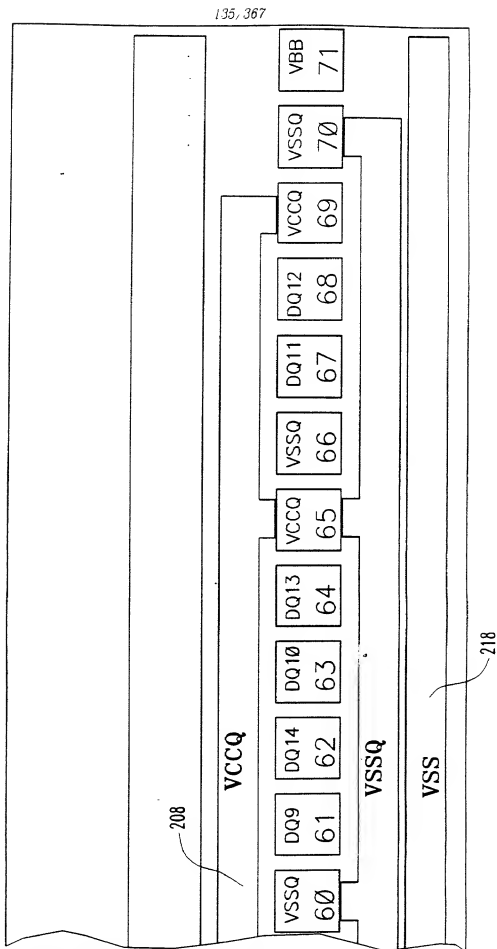


FIG. 34C2

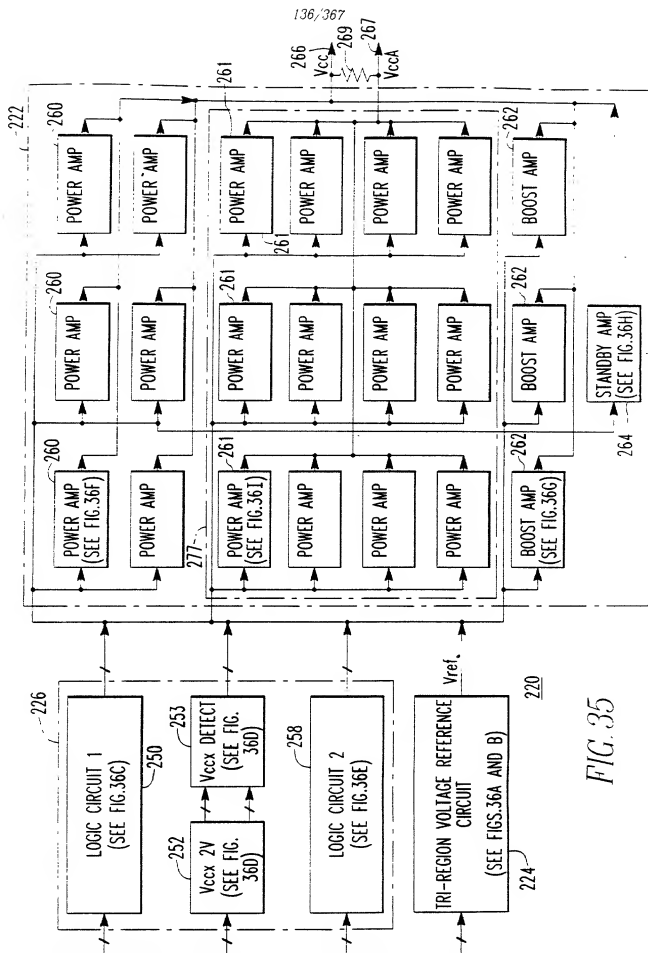


FIG. 35

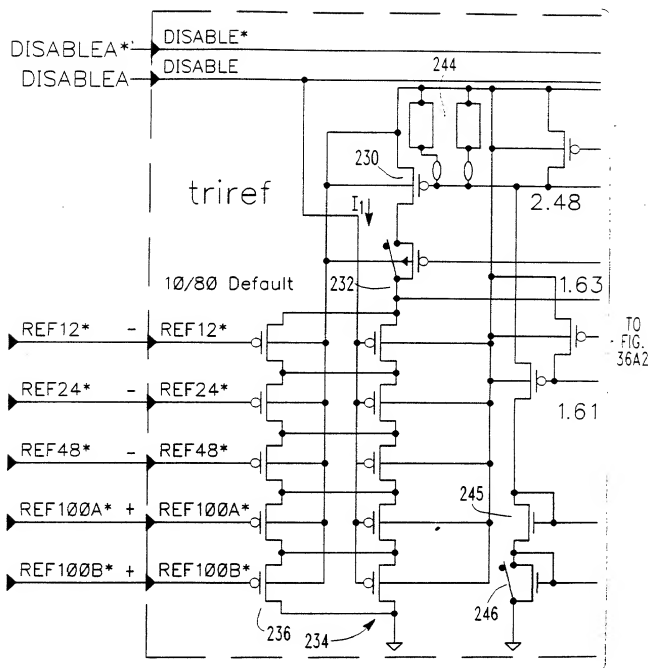


FIG. 36A1

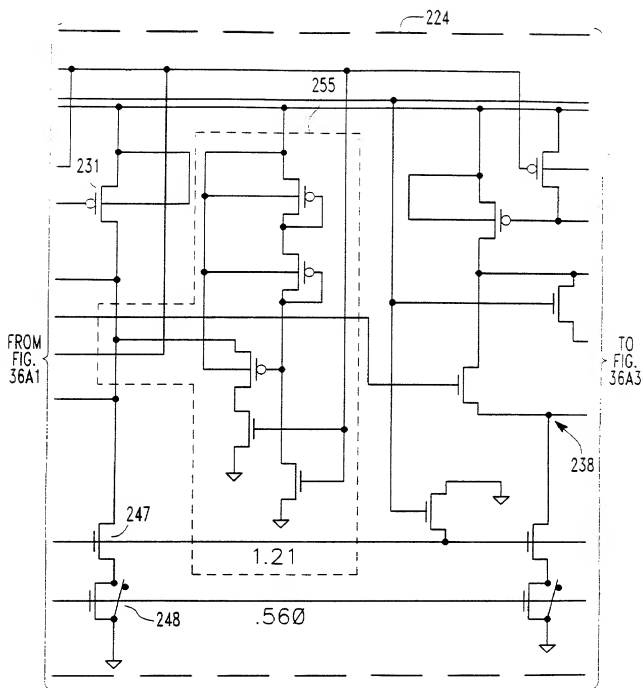


FIG. 36A2

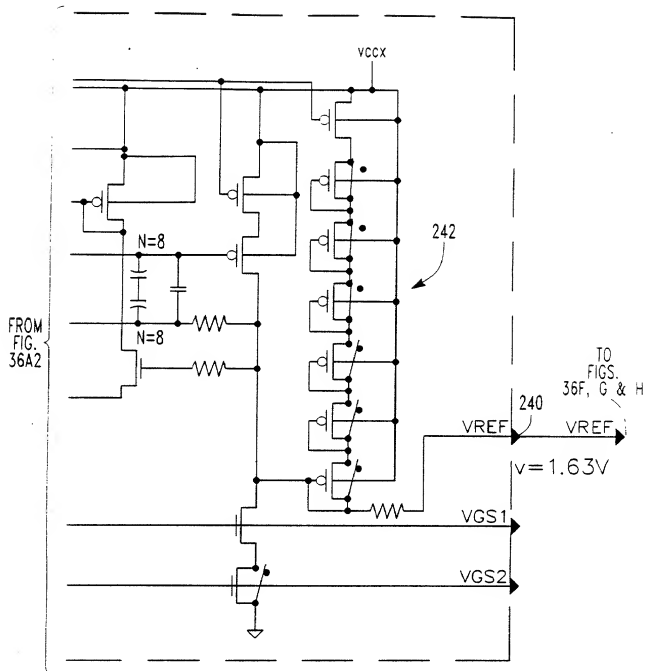


FIG. 36A3

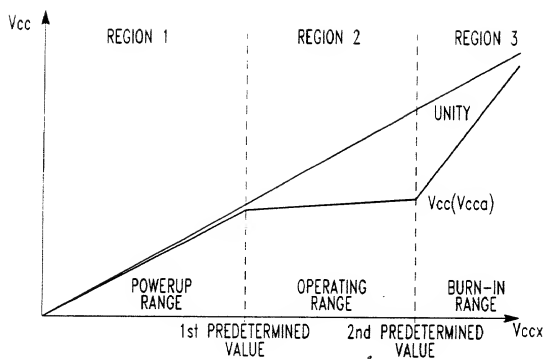


FIG. 36B

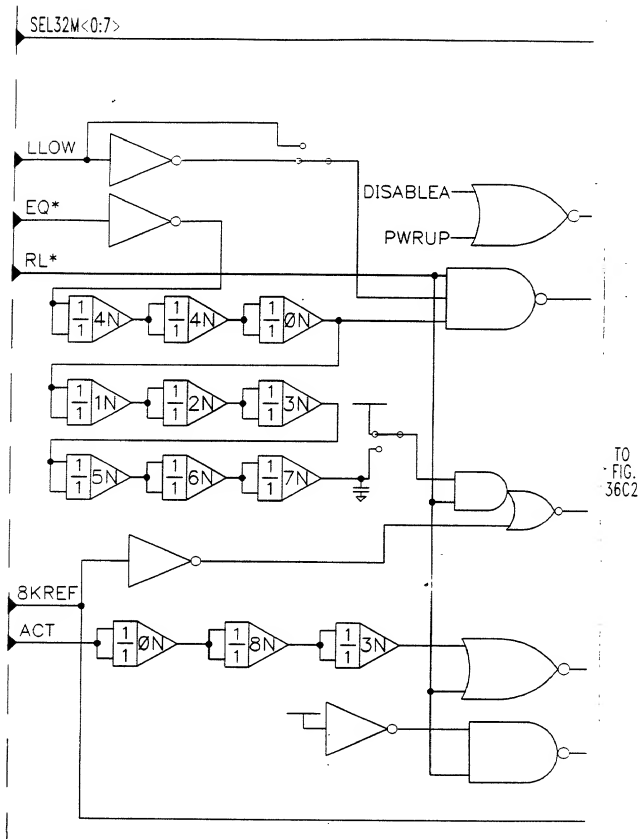


FIG. 36C1

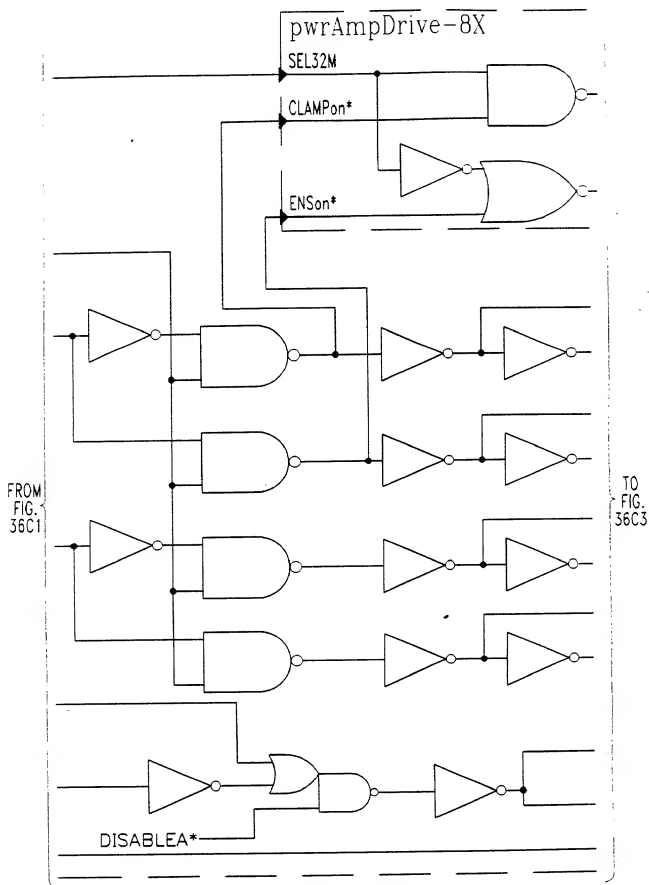


FIG. 36C2

143/367

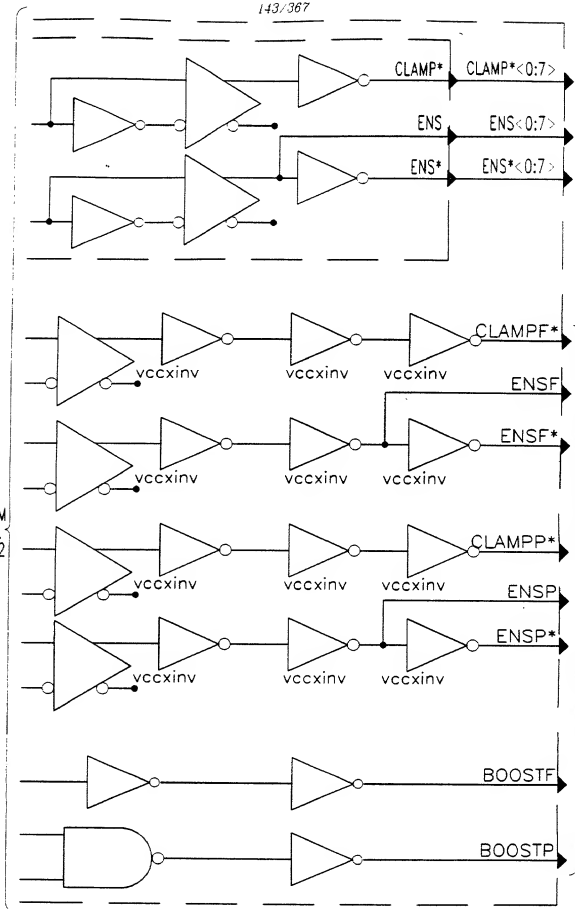
FROM
FIG.
36C2TO
FIG.
36F

FIG. 36C3

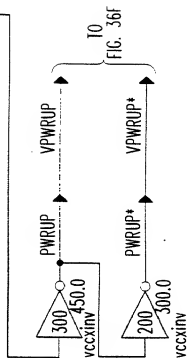
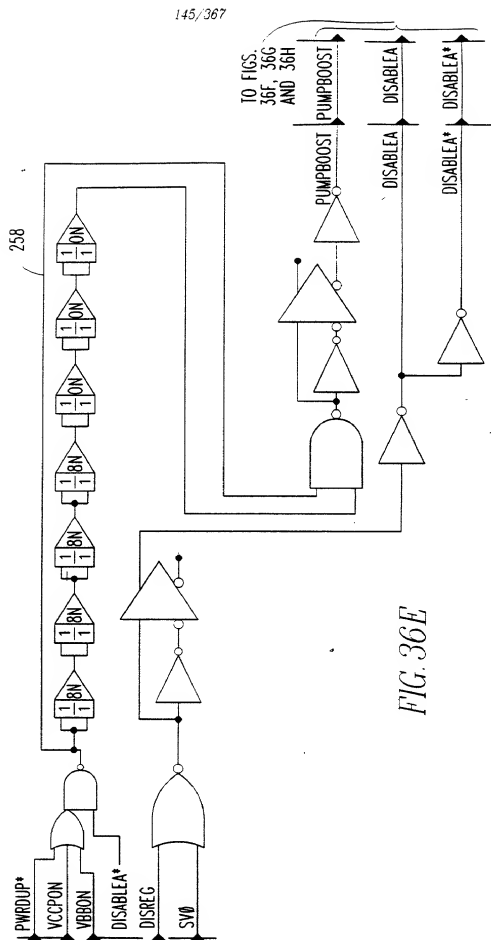


FIG. 36D



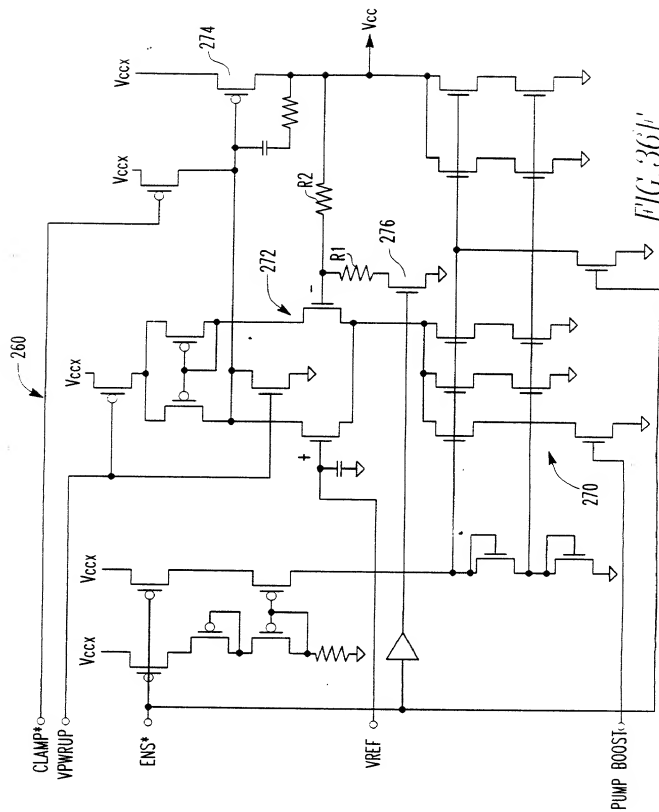


FIG. 36F

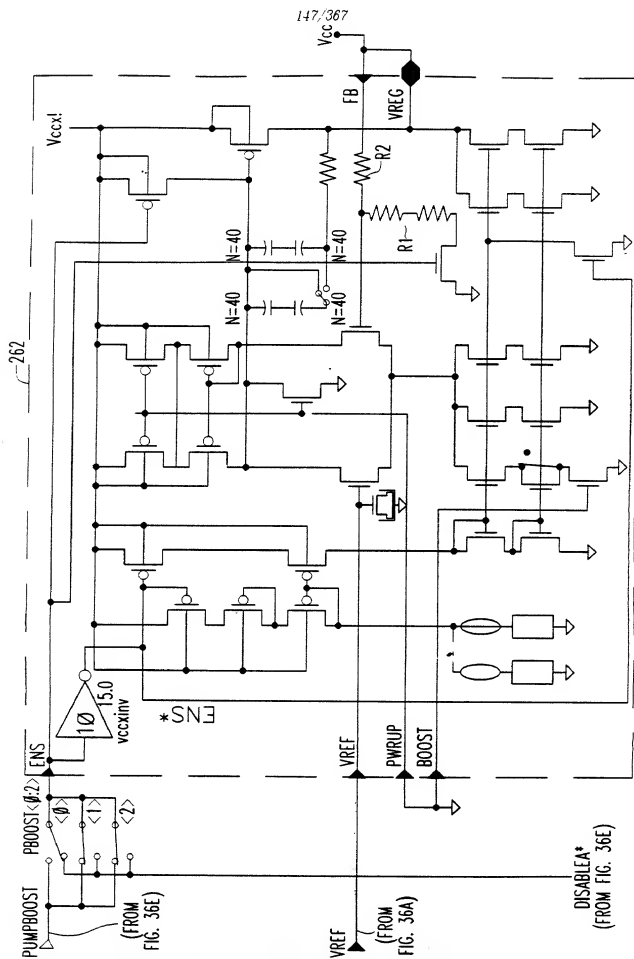
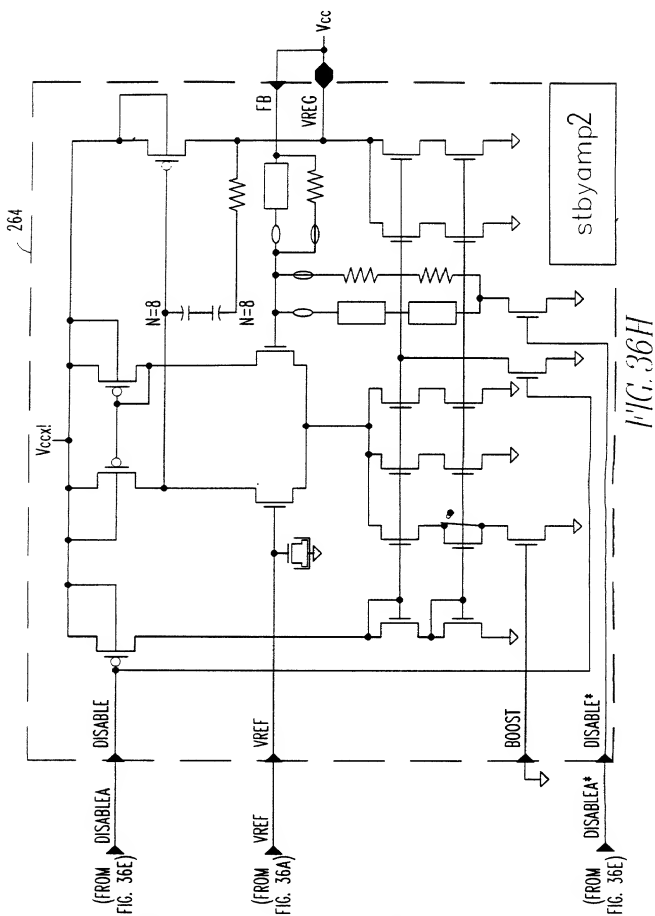
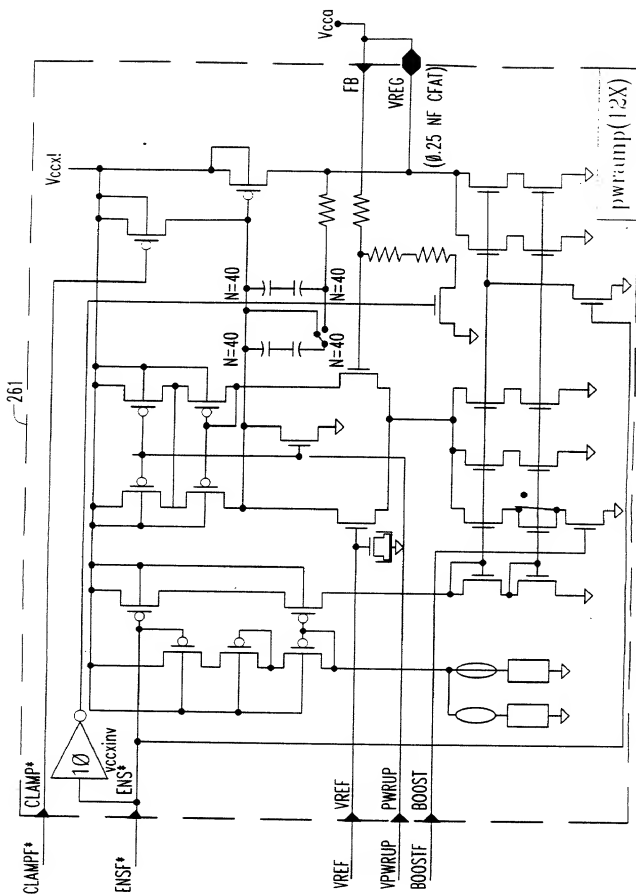


FIG. 36G





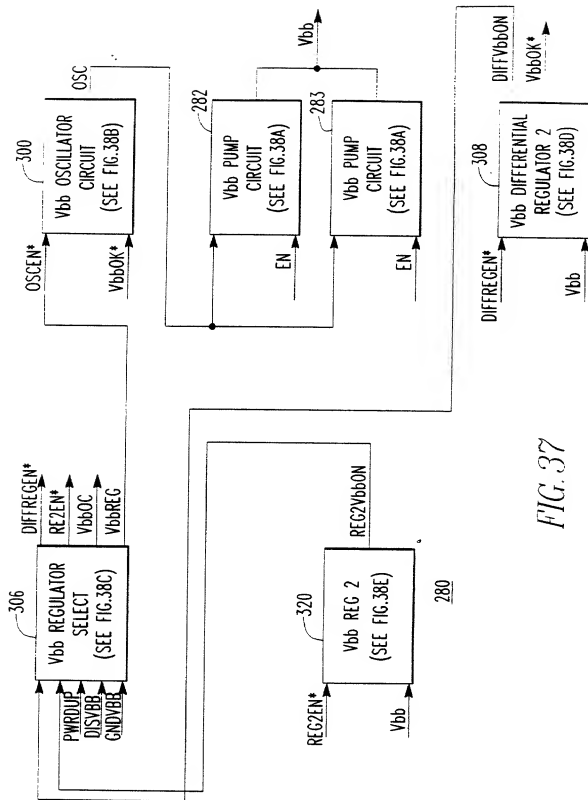


FIG. 37

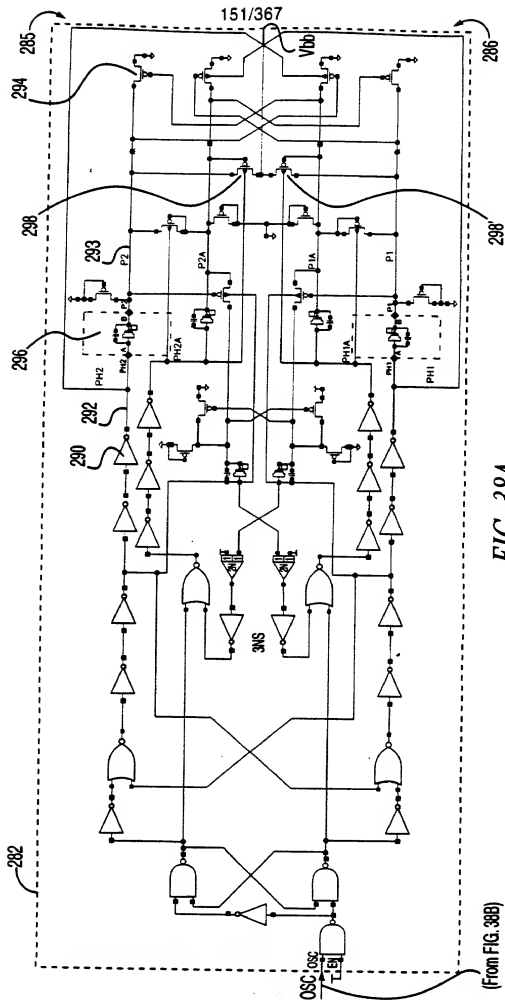


FIG. 38A

(From FIG. 38B)